Boot from Serial RapidIO™/PCI Express™ on PowerQUICC™ III and QorIQ™ P1xx/P2xx

by Freescale Semiconductor, Inc.
Austin, TX

This document is an overview of how to configure PowerQUICC III and QorIQ P1xx/P2xx devices to boot from serial RapidIO™ or PCI Express™ with no additional boot flash/EEPROM. The MPC8572E is used as an example but the description is generally applicable with small changes (for example, the number of CPU cores or cache size of the device). Use the PowerQUICC™ III MPC8572E Integrated Host Processor Family Reference Manual (MPC8572ERM) and related documentation for more in-depth information. The recommended configurations should be double-checked with the appropriate reference manual to verify the intended boot scenario.

1 Overview

The boot scenario this application note describes is a device acting as an agent/endpoint under a controlling host. This host could be another processor, FPGA, etc. As the MPC8572E is powered up, it can follow two different scenarios for booting, as follows:

1. The MPC8572E is set to run the boot loader over a memory-mapped interface handled by the host unit. This boot program can then configure DDR and other interfaces, shown in Figure 1.
2. The MPC8572E executes a boot program from local DDR. The host must configure the DDR controller, upload a boot program to DDR, and then let it execute from there, shown in Figure 2.

There is no RAM/ROM directly connected to the MPC8572E involved in either of the two boot procedures.

2 Power-On Sequence

The basic power-on sequence is listed in Section 4.4.2, “Power-On Reset Sequence,” in the PowerQUICC™ III MPC8572E Integrated Host Processor Family Reference Manual.

3. In short, the following takes place:
   a) Apply power.
   b) HRESET and TRST (JTAG interface, Test Reset) resets registers and I/O.
   c) Clock and PLL synchronization occurs.
   d) Release HRESET.
   e) I/O drivers are enabled.
   f) Core PLLs lock on device clock.
   g) Internal hard reset to core and peripherals are released.

4. If enabled, the boot sequencer starts. This is not desired because it will try to boot from I²C. For boot using PCI Express or serial RapidIO, the boot sequencer should be disabled. Ensure that cfg_boot_seq[0:1] is set to “11” (disabled) as its default values. See Section 4.3.2, “Boot Sequencer,” in the PowerQUICC™III MPC8572E Integrated Host Processor Family Reference Manual.

5. The serial RapidIO and PCI Express interfaces begin training. Ensure the ports are properly configured and cfg_IO_ports[0:3] is configured based on your needs (see Section 4.4.3.6, “I/O Port Selection,” in the PowerQUICC™ III MPC8572E Integrated Host Processor Family Reference Manual for details). Also ensure that clocks and other interface-specific needs are handled.
6. Serial RapidIO and PCI Express interfaces are released to accept external requests. Ensure that
    \( \text{cfg\_host\_agt[0]:2} \) is configured to allow for external host configuration, for example “000.” This
    is not the default value. See Section 4.4.3.5, “Host/Agent Configuration,” in the PowerQUICC™

7. Point the boot memory to the appropriate location. For scenario 1 (shown in Figure 1), this is
    DDR memory, and for scenario 2 (shown in Figure 2), this is the serial RapidIO/PCI Express
    interface. Default “Boot ROM” address the interface must respond as needed is an 8-Mbyte
    interval ranging from 0xFF80_0000 to 0xFFFF_FFFF. Ensure that \( \text{cfg\_rom\_loc[0]:3} \) is correctly
    set depending on boot location. See Section 4.4.3.4, “Boot ROM Location” in the

8. The e500 cores are now ready to start execution from the reset vector. Because no program is
    available from Flash/ROM, this is currently not desired. Further boot should therefore be
    prevented, this is done by setting the cores in “hold off” mode using POR configuration inputs.
    Ensure that \( \text{cfg\_cpu0\_boot} \) and \( \text{cfg\_cpu1\_boot} \) is set to “00” to prevent cores from booting until
    configured by external master. (In single core devices this will be called \( \text{cfg\_cpu\_boot} \). These are
    not default values. See Section 4.4.3.7, “CPU Boot Configuration,” for more information.

9. The MPC8572E is now in its ready state and accepts external configuration. Configurations
    typically consist of the following:
    a) An MMU page with a 4-Kbyte interval is initially set per core to address 0xFFFF_Fnnn. This
        window can be changed by altering the boot page translation register. See Section 9, “Boot
        Page Translation.”

    **NOTE**
    The page translation must be within the “Boot ROM” interval
    (0xFF80_0000 to 0xFFFF_FFFF) or a local access window (LAW) must be
    added in addition.

    b) In case of scenario 2, the host must configure DDR controller or alternatively configure L2
        cache as SRAM, and upload the program to it. Configuring the L2 cache as SDRAM is
        described in Section 3, “Configuring L2 Cache as SRAM.”

10. Once the device is configured and a boot loader is pointed to the reset vector, the cores can be
    released. The first instruction is located on instruction 0xFFFF_FFFC with the first instruction
    fetch to address 0x0FFFF_FFE0. Two approaches are possible. Alternatively, the external host
    only releases one core that continues initialization, and then when ready, releases the other core.
    The cores are released, both by an external host as well as by another core, by changing the values
    of CPU\(_n\)\_EN. This register is described in Section 8.2.1.2, “ECM CCB Port Configuration
    Register (EEBPCR)” of the PowerQUICC™ III MPC8572E Integrated Host Processor Family
    Reference Manual. The POR status can be acquired from the PORBMSR register (see section
    23.4.1.2 “POR Boot Mode Status Register (PORBMSR)”).

11. The ASLEEP signal negates synchronized to a rising edge of SYSCLK, indicating the ready state
    of the system. The ready state for e500 core \( n \) is also indicated by the assertion of
    READY\(_Pn\)/TRIG\_OUT. The assertion of READY\(_P0\) and READY\(_P1\) allows external system
    monitors to know basic device status, for example, exactly when each e500 core emerges from
reset, or if the particular core is in a low-power mode. Section 4.4.2, “Power-On Reset Sequence,” in the *PowerQUICC™ III MPC8572E Integrated Host Processor Family Reference Manual* describes this further.

12. The boot loader is now executing.

Figure 3 shows the power-on reset sequence.

![Power-On Reset Sequence Diagram](image)

### Figure 3. Power-On Reset Sequence

#### 3 Configuring L2 Cache as SRAM

The L2 cache can be mapped in part or as a whole into SRAM and used for program and/or data storage. This is done on a per way basis. For initial boot, as is the case here, it is easiest to map the whole cache as SRAM. Once the bootloader is running from DDR or over PCI-E/sRIO interface the cache can be set back to normal operation.

The cache is configured and enabled using the L2CTL register. For example, on an MPC8572E, the value 0xB001_0000 is written into the L2CTL located at address 0xFF72_0000. The new memory also needs a base address assigned and this is done by changing the L2SRBAR0 register. Because the MPC8572E has 1 Mbyte of cache and the last bytes of the 32-bit memory region should be covered, ending at 0xFFFF_FFFF. Set the base address to be 0xFFF0_0000, which is done by writing 0xFFF0_0000 into the register located at 0xFF72_0100.
Because this memory region is covered by a default LAW at power-on reset, it does not have to be added. The memory is now ready to be used. Memory mapping collisions with external memory or flash should not be seen because the L2 cache takes precedence.

4 Boot Debugging Using JTAG

Debugging PCI-E/sRIO-based booting can be seen as more complex because there is little access to the device before all configurations have taken place. It can be useful to fall back to the JTAG interface for board bring-up and verifying memory configurations, and ensuring that the cores come out of reset etc. However, this can be an issue because many debuggers have issues dealing with the facts that the device is in hold-off mode and it does not have any memory mapped to the reset register. The latter is solved by mapping the cache as memory as described in Section 3, “Configuring L2 Cache as SRAM.”

To simplify JTAG-based debugging, the following initialization script can be used with the Freescale CodeWarrior debugger, replacing the first section of the standard init files. Similar scripts should work on other tools as well. This script ends with a Run, Sleep, Stop command chain. This is because the e500 core must run before any debug instruction can be sent to it, which is done by setting a hard breakpoint at the reset vector and start execution. The core starts fetching instructions to fill the pipeline but never executes the instruction before the breakpoint is hit. However, it is required that there is a legal instruction at the reset vector as well as at the debug and program exception; the script handles this by writing the OP code 0x4800_0000.

The default initialization scripts also contains a Run, Sleep, Stop chain, this marks where the default scripts should continue from the one provided as follows:

```
########################################################################################
# Initialization file for MPC8572E using L2 Cache as SRAM and clearing hold-off mode.
########################################################################################

writemem.l 0xFF720000 0xB0010000  # enable L2 as SRAM
writemem.l 0xFF720100 0xFFF00000  # set L2 SR BAR
writemem.l 0xFFFFF000 0x48000000 # instruction at debug interrupt
writemem.l 0xFFFFF700 0x48000000 # instruction at program interrupt
writemem.l 0xFFFFFFFC 0x48000000 # instruction at reset vector

# set interrupt vectors
writereg IVPR  0xFFFF0000 # IVPR (pointing to L2 SRAM location)
writereg IVOR15 0x0000F000 # debug - (a valid instruction should exist to be fetched)
writereg IVOR6  0x0000F700 # program
```

Boot Debugging Using JTAG
## CPU Boot Configuration

The CPU boot configuration inputs shown in Table 1 specify the boot configuration mode. If $\text{LA}[27]/\text{EC3}_\text{MDC}$ are set low at reset, then core 0/core 1 does not execute code until released by an external master. This is done by setting the ECM CCB port configuration register bit $\text{EEBPCR}[\text{CPU0}_\text{EN}]$ for core 0 and $\text{EEBPCR}[\text{CPU1}_\text{EN}]$ for core 1.

The values sampled at power-on reset are accessible through the POR boot mode status register. This also affects the “configuration ready mode” on PCI Express interfaces. See Section 4.4.3.7, “CPU Boot Configuration,” in the *PowerQUICC™ III MPC8572E Integrated Host Processor Family Reference Manual* for more information.

Table 1 shows the CPU boot configuration.

### Table 1. CPU Boot Configuration

<table>
<thead>
<tr>
<th>Functional Signal</th>
<th>Reset Configuration Name</th>
<th>Value (Binary)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\text{LA}[27]$, $\text{EC3}_\text{MDC}$</td>
<td>$\text{cfg}<em>\text{cpu0}</em>\text{boot}$, $\text{cfg}<em>\text{cpu1}</em>\text{boot}$</td>
<td>00</td>
<td>CPU boot holdoff mode for both cores. The e500 cores are prevented from booting until configured by an external master.</td>
</tr>
<tr>
<td>Default (11)</td>
<td></td>
<td>01</td>
<td>e500 core 1 is allowed to boot without waiting for configuration by an external master, while e500 core 0 is prevented from booting until configured by an external master or the other core.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>e500 core 0 is allowed to boot without waiting for configuration by an external master, while e500 core 1 is prevented from booting until configured by an external master or the other core.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11</td>
<td>Both e500 cores are allowed to boot without waiting for configuration by an external master (default).</td>
</tr>
</tbody>
</table>
## 6 Host/Agent Configuration

The host/agent reset configuration shown in Table 2 selects if the MPC8572E should be acting as host/root complex or agent/endpoint.

The values sampled at power-on reset are accessible through the POR boot mode status register. See Section 4.4.3.5, “Host/Agent Configuration,” in the *PowerQUICC™ III MPC8572E Integrated Host Processor Family Reference Manual* for additional information.

Table 2 shows the host/agent configuration.

### Table 2. Host/Agent Configuration

<table>
<thead>
<tr>
<th>Functional Signals</th>
<th>Reset Configuration Name</th>
<th>Value (Binary)</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| LWE[1:3]/LBS[1:3]  | cfg_host_agt[0:2]       | 000            | PCI Express 1: endpoint  
                               PCI Express 2: endpoint  
                               PCI Express 3: endpoint  
                               Serial RapidIO: agent |
| Default (111)      |                         | 001            | PCI Express 1: endpoint  
                               PCI Express 2: root complex  
                               PCI Express 3: root complex  
                               Serial RapidIO: host |
|                    |                         | 010            | PCI Express 1: root complex  
                               PCI Express 2: endpoint  
                               PCI Express 3: root complex  
                               Serial RapidIO: agent |
|                    |                         | 011            | PCI Express 1: root complex  
                               PCI Express 2: root complex  
                               PCI Express 3: endpoint  
                               Serial RapidIO: host |
|                    |                         | 100            | PCI Express 1: endpoint  
                               PCI Express 2: endpoint  
                               PCI Express 3: root complex  
                               Serial RapidIO: agent |
|                    |                         | 101            | PCI Express 1: endpoint  
                               PCI Express 2: root complex  
                               PCI Express 3: endpoint  
                               Serial RapidIO: host |
|                    |                         | 110            | PCI Express 1: root complex  
                               PCI Express 2: endpoint  
                               PCI Express 3: endpoint  
                               Serial RapidIO: agent |
|                    |                         | 111            | PCI Express 1: root complex  
                               PCI Express 2: root complex  
                               PCI Express 3: root complex  
                               Serial RapidIO: host |
## 7 I/O Port Configuration

The configurations in Table 3 show possible combinations of IO ports and bit rates for serial RapidIO and PCI Express interfaces on the MPC8572E. See Section 4.4.3.6, “I/O Port Selection,” in the *PowerQUICC™ III MPC8572E Integrated Host Processor Family Reference Manual* for additional information.

Table 3 shows the I/O port selection.

**Table 3. I/O Port Selection**

<table>
<thead>
<tr>
<th>Functional Signal</th>
<th>Reset Configuration Name</th>
<th>Value (Binary)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSEC1_TXD[3:1], TSEC2_TX_ER Default (1111)</td>
<td>cfg_IO_ports[0:3]</td>
<td>0000</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0001</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
| | | 0010 | PCI Express 1 (x4) (2.5 Gbps)  
100-MHz reference clock  
RX lane[0:3] -> SD1_RX[0:3]  
TX lane[0:3] -> SD1_TX[0:3] |
| | | 0011 | PCI Express 1 (x4) (2.5 Gbps), PCI Express 2 (x4) (2.5 Gbps)  
100-MHz reference clock  
PCI Express 1:  
RX lane[0:3] -> SD1_RX[0:3]  
TX lane[0:3] -> SD1_TX[0:3]  
PCI Express 2:  
RX lane[0:3] -> SD1_RX[4:7]  
TX lane[0:3] -> SD1_TX[4:7] |
| | | 0100 | Reserved |
| | | 0101 | Reserved |
| | | 0110 | Serial RapidIO x4 (2.5 Gbps)  
100 MHz reference clock  
RX lane[0:3] -> SD1_RX[4:7]  
TX lane[0:3] -> SD1_TX[4:7] |
| | | 0111 | PCI Express 1 (x4), PCI Express 2 (x2), PCI Express 3 (x2)  
100-MHz reference clock  
PCI Express 1:  
RX lane[0:3] -> SD1_RX[0:3]  
TX lane[0:3] -> SD1_TX[0:3]  
PCI Express 2:  
RX lane[0:1] -> SD1_RX[4:5]  
TX lane[0:1] -> SD1_TX[4:5]  
PCI Express 3:  
RX lane[0:1] -> SD1_RX[6:7]  
TX lane[0:1] -> SD1_TX[6:7] |
8 Boot ROM Location

The default memory window at boot is an 8-Mbyte block at physical address 0xFFFF0_0000–0xFFFF_FFFF. This area is open to a specific interface and Table 4 shows how this interface is selected.

Note that a 4-Kbyte MMU entry is also set at boot time; see Section 9, “Boot Page Translation.” It is important that the MMU entry and the boot ROM location overlap, or a new local address window (LAW) must be configured. See Section 4.4.3.4, “Boot ROM Location,” in the PowerQUICC™ III MPC8572E Integrated Host Processor Family Reference Manual for additional information.
Table 4 shows the boot ROM location.

### Table 4. Boot ROM Location

<table>
<thead>
<tr>
<th>Functional Signals</th>
<th>Reset Configuration Name</th>
<th>Value (Binary)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSEC1_TXD[6:4],</td>
<td>cfg_rom_loc[0:3]</td>
<td>0000</td>
<td>PCI Express 1</td>
</tr>
<tr>
<td>TSEC1_TX_ER</td>
<td></td>
<td>0001</td>
<td>PCI Express 2</td>
</tr>
<tr>
<td>Default (1111)</td>
<td></td>
<td>0010</td>
<td>Serial RapidIO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0011</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0100</td>
<td>DDR controller 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0101</td>
<td>DDR controller 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0110</td>
<td>DDR Interleaved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0111</td>
<td>PCI Express 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1000</td>
<td>Local bus FCM—8-bit NAND Flash small page</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1001</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1010</td>
<td>Local bus FCM—8-bit NAND Flash large page</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1011</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1100</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1101</td>
<td>Local bus GPCM—8-bit ROM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1110</td>
<td>Local bus GPCM—16-bit ROM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1111</td>
<td>Local Bus GPCM—32-bit ROM (default)</td>
</tr>
</tbody>
</table>

### 9 Boot Page Translation

At boot time, each core has a 4-Kbyte MMU entry set to address 0xFFFF_Fxxx with the first instruction executed at address 0xFFFF_FFFC. The boot translation register allows for remapping of this location, which affects both cores. This can either be initiated from the boot sequencer or alternatively, when starting the cores in hold-off mode, it can be configured from an external host.

Note that a 4-Kbyte MMU entry is also set at boot time. It is important that the MMU entry and the boot ROM location overlap, or a new local address window (LAW) must be configured. See Section 4.3.1.3, “Boot Page Translation,” in the PowerQUICC™ III MPC8572E Integrated Host Processor Family Reference Manual for more details.

Table 5 defines the BPTR fields.

### Table 5. BPTR Bit Settings

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>EN</td>
<td>Boot page translation enable for e500 core transactions</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Boot page is not translated.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Boot page is translated as defined in the BPTR[BOOT_PAGE] parameter.</td>
</tr>
<tr>
<td>1–7</td>
<td>—</td>
<td>Write reserved, read = 0</td>
</tr>
<tr>
<td>8–31</td>
<td>BOOT_PAGE</td>
<td>Translation for boot page. If enabled, the high order 24 bits of e500 core accesses to 0x0_FFFF_Fnnn are replaced with this value.</td>
</tr>
</tbody>
</table>
10 Boot Sequencer Configuration

The boot sequencer allows for boot code to be loaded from an external memory through the \( I^2C1 \) port. If this is not desired it should be disabled at boot time.

The values sampled at power-on reset are accessible through the POR boot mode status register. See Section 4.3.2, “Boot Sequencer,” in the *PowerQUICC™ III MPC8572E Integrated Host Processor Family Reference Manual* for more information.

Table 6 shows the boot sequencer configuration.

<table>
<thead>
<tr>
<th>Functional Signal</th>
<th>Reset Configuration Name</th>
<th>Value (Binary)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>LGPL3/LFWP, LGPL5</td>
<td>cfg_boot_seq[0:1]</td>
<td>00</td>
<td>Reserved</td>
</tr>
<tr>
<td>Default (11)</td>
<td></td>
<td>01</td>
<td>Normal ( I^2C ) addressing mode is used. Boot sequencer is enabled and loads configuration information from a ROM on the ( I^2C1 ) interface. A valid ROM must be present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>Extended ( I^2C ) addressing mode is used. Boot sequencer is enabled and loads configuration information from a ROM on the ( I^2C1 ) interface. A valid ROM must be present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11</td>
<td>Boot sequencer is disabled. No ( I^2C ) ROM is accessed (default).</td>
</tr>
</tbody>
</table>

11 Revision History

Table 7 provides a revision history for this application note.

<table>
<thead>
<tr>
<th>Rev. Number</th>
<th>Date</th>
<th>Substantive Change(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>10/2009</td>
<td>Initial public release.</td>
</tr>
</tbody>
</table>
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