Introduction to the Plastic Ball Grid Array (PBGA)

Q1, 2008
Presentation Outline

PBGA Introduction and Package Description
PC Board Design for PBGA
PBGA Assembly
PBGA Solder Joint Voids
Rework
Solder Joint Reliability
Thermal Performance
## Package Terminology

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PBGA</td>
<td>Plastic Ball Grid Array; Can be either 2 layer or 4 layer substrates; BGA pitch range from 1.0-1.27mm; Body size &gt;23mm x 23mm</td>
</tr>
<tr>
<td>TEPBGA</td>
<td>Thermally Enhanced PBGA; 4 layer substrate with 2oz Cu inner layers for increased thermal performance</td>
</tr>
<tr>
<td>TEPBGA-2</td>
<td>Thermally Enhanced PBGA with Embedded Heatspreader; TEPBGA plus heatspreader over die</td>
</tr>
<tr>
<td>MAP</td>
<td>Mold Array Package; A type of PBGA, except mold cap covers entire topside surface; BGA pitch range from 0.5-1.0mm; Body size &lt;19mm x 19mm</td>
</tr>
</tbody>
</table>

PBGA >= 23x23  
MAP <= 19x19
PBGA Introduction and Package Description

PBGA BGA Construction

“MAP” Style
PBGA Molded to Substrate Edge

Die Attach

Silicon Die

Au Bond Wires

Epoxy Overmold

Substrate with Soldermask

Joint Stand-Off
(Varies with Pad Sizes, Sphere Sizes and Solder Paste Volume)

Motherboard

Ball Pitch

Solder Sphere

Solder Pads (PBGA Package Pads - PCB Pad)

Thermal and/or Ground Vias

Routing Vias
PBGA Introduction and Package Description

Typical Plastic Ball Grid Array
(416 Pin, 1.0 mm Pitch, 27x27 mm sq.)
MAP Introduction and Package Description

Typical MAP Ball Grid Array
(196 Pin, 1.0 mm Pitch, 15x15 mm sq.)
PBGA Introduction and Package Description

PBGA s ship with one of several sphere compositions depending if they are Pb-free or lead-containing
  • All PBGA spheres should collapse during assembly to PCB
  • Collapse is controlled by pad geometries on package and PCB and solder surface tension

Lead containing sphere compositions:
  • The most common is 62Sn36Pb2Ag
  • Some may contain 63Sn37Pb

Lead-free sphere compositions:
  • The most common is 95.5Sn4.0Ag0.5Cu, commonly called SAC405
  • Devices used in handheld applications may use SAC105 (98.5Sn1Ag0.5Cu)
  • Some parts may contain 96.5Sn3.5Ag
PBGA Introduction and Package Description

Solder alloy melting temperatures:

<table>
<thead>
<tr>
<th>Composition (Weight %)</th>
<th>95.5Sn4.0Ag0.5Cu (SAC405)</th>
<th>98.5Sn1.0Ag0.5Cu (SAC105)</th>
<th>96.5Sn3.5Ag</th>
<th>62Sn36Pb2Ag</th>
<th>63Sn37Pb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solidus (°C)</td>
<td>217</td>
<td>215</td>
<td>221</td>
<td>179</td>
<td>183</td>
</tr>
<tr>
<td>Liquidus (°C)</td>
<td>224</td>
<td>227</td>
<td>221</td>
<td>189</td>
<td></td>
</tr>
</tbody>
</table>

References:
http://www.pbfree.com/alloys.php
http://www.boulder.nist.gov/div853/lead%20free/props01.html
PBGA Advantages

BGA: Ideal interconnect technology

- Using solder spheres as leads:
  - Provides perfect self alignment
  - Allows large tolerance in placement accuracy
  - Eliminates lead coplanarity issues
  - Allows high number of I/O connections with large pitch
    - Large savings in board real-estate
    - Offers electrical and thermal advantages
- SMT manufacturing processes simplified
- SMT manufacturing equipment demands less stringent
- SMT manufacturing yields dramatically improved versus fine pitch leaded parts
Presentation Outline

PBGA Introduction and Package Description
PC Board Design for PBGA
  • Pad Diameter
PBGA Assembly
PBGA Solder Joint Voids
Rework
Solder Joint Reliability
Thermal Performance
PC Board Design for PBGA

For PBGA, both PC board solder pad and stencil aperture diameters should generally be made 1:1 with the package solder pad diameter.

Stencil thickness is typically dependent on other components on the PCB such as fine pitch leaded and discretes:
- 0.10 to 0.20 mm thick stencils are commonly used with PBGA.
- In some cases such as larger body size PBGAs, a thicker stencil may provide improved assembly robustness.

Package pad diameters are generally one half the pitch, but can vary slightly on some products – check with Freescale or your distributor if there are questions.

Below is a table of some typical PBGA pad diameters:

<table>
<thead>
<tr>
<th>Ball Pitch</th>
<th>Package Pad Dia.</th>
<th>PCB Pad Dia. (1)</th>
<th>Stencil Opening Dia. (2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.27</td>
<td>0.635</td>
<td>0.635</td>
<td>0.635</td>
</tr>
<tr>
<td>1.00</td>
<td>0.40 to 0.50</td>
<td>0.40 to 0.50</td>
<td>0.40 to 0.50</td>
</tr>
<tr>
<td>0.80</td>
<td>0.40</td>
<td>0.40</td>
<td>0.40</td>
</tr>
<tr>
<td>0.65</td>
<td>0.3 to 0.325</td>
<td>0.3</td>
<td>0.3</td>
</tr>
<tr>
<td>0.50</td>
<td>0.25 to 0.3</td>
<td>0.25 to 0.3</td>
<td>0.25 to 0.3</td>
</tr>
</tbody>
</table>

Note:
(1) Studies have shown that PCB pad diameters up to approximately 10% smaller than the package pad still provides good board-level thermal cycling reliability. A PC board solder pad that is of greater diameter than the package pad is not recommended.
(2) General industry practice for PBGA has stencil opening diameter equal to PCB pad diameter.
SMD vs NSMD PCB Pads for PBGA

There are two types of PCB pad configurations for PBGA:

- SolderMask Defined pads (SMD) which are the type on the PBGA itself
- Non-SolderMask Defined (NSMD) or Cu defined pads are most commonly used on PC boards within the industry

Comparison of PC board SMD (left) and NSMD (right) pads shown with OSP (OSP or organic solderability protectant) surface finish.

Besides the OSP shown above, there are many surface finishes available: HASL, Immersion Ag, ENIG, etc….
Trade-Offs Between SMD and NSMD PCB Pads for PBGA

**SMD = SolderMask Defined**

**Advantage**
1. Strongest mechanical strength
2. More copper, better heat spreading to board
3. More heat resistant - multiple rework

**Disadvantages**
1. Potential stress point
2. Foreign matter entrapment on pad
3. Possible worse dimensional tolerance on solderable diameter versus NSMD

**NSMD = Non-SolderMask Defined**

**Advantages**
1. Most common pad configuration
2. Potentially the most solderable pad
3. No point of stress concentration at PCB board
4. More copper to copper space to route traces between pads

**Disadvantages**
1. Reduced pad to PCB adhesion strength
2. May be weak link in other mechanical testing, i.e. board bending, mechanical shock and vibration
3. Non-symmetrical joint fails at the package interface first in thermal cycling
PCB Pad Design Guidelines

General PCB Pad Dimensions

- Pad solderable diameter equal to package pad diameter
  - Smaller PC board pad diameter by approximately 10% may ease routing and still provide good reliability
- NSMD pads - soldermask opening 0.125 mm > pad diameter
- SMD pads - Cu pad area 0.125 mm > soldermask opening
- Surface finishes include: organic solderability protectant (OSP), HASL, electroless or electrolytic nickel/gold (NiAu), or immersion silver (Ag)

PCB Routing Vias

- For 1.27, 1.0 and 0.8 mm pitches, via interstitial between BGA pads
  - Via Cu capture pad set by drill size of via
  - Capture pad usually tented with solder mask
  - Trace between pad and capture pad should be covered with soldermask
    - Too small a width of soldermask can lead to soldermask lift off the trace
- For 0.8, 0.65 and 0.50 mm pitches, via-in-pad structures
  - Via is part of BGA pad
  - Filled via best for void minimization of final solder-joint
  - Contact PCB fabrication vendors for manufacturing capability
    - Laser or mechanical drilling, as appropriate
    - Size of drill hole for via
    - Through-hole via or single layer via
PCB Pad Design

- Finished Plated Through Hole
- Annular Capture Pad
- Soldermask
- Copper Solder Pad
- Clearance Between Copper and Soldermask
- Soldermask Away From Copper Pad
- PCB Laminate
- Cross Section
- Via
- Solder Pad
- Top View
- Offset Via Example
- Via-in-Pad Example
- Solder Pad
- Top View
- Via-in-Pad May be filled
- Cross Section
Presentation Outline

PBGA Introduction and Package Description
PC Board Design for PBGA
PBGA Assembly
  • Pre-assembly Handling
  • Placement and Reflow
  • Secondary Reflow
  • Cleaning and Inspection
PBGA Solder Joint Voids
Rework
Solder Joint Reliability
Thermal Performance
**PBGA Pre-Assembly Handling: Moisture Sensitivity**

Similar to QFP and other leaded and leadless plastic packages, most PBGAs are generally moisture sensitive

- Follow moisture sensitivity guidelines printed on the package dry-pack label
- Check the label for maximum allowable reflow temperature for product

### Jedec Moisture Level Table

<table>
<thead>
<tr>
<th>MSL Level</th>
<th>Floor Life</th>
<th>Storage Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Unlimited</td>
<td>30C/85%RH</td>
</tr>
<tr>
<td>2</td>
<td>1 Year</td>
<td>30C/60%RH</td>
</tr>
<tr>
<td>2a</td>
<td>4 Weeks</td>
<td>30C/60%RH</td>
</tr>
<tr>
<td>3</td>
<td>168 Hours</td>
<td>30C/60%RH</td>
</tr>
<tr>
<td>4</td>
<td>72 Hours</td>
<td>30C/60%RH</td>
</tr>
<tr>
<td>5</td>
<td>48 Hours</td>
<td>30C/60%RH</td>
</tr>
</tbody>
</table>

**Source:** JEDEC JESD22-A113

Floor life is the time allowed out of dry-pack before a rebake is required.
PBGA Pre-Assembly Handling: Moisture Sensitivity

Easy to avoid PBGA package delamination

- Follow instructions on shipping container
- Establish strict process control and procedures to insure safe operation conditions.
  - Use dry nitrogen or dessicator cabinets to store devices after opening packages
- Rework boards within time allowed in room environment
- Failure to follow MSL guidelines can result in package failure.
Solder Paste Printing for PBGA

Solder paste stencil thicknesses generally range from 0.10 to 0.20 mm. Stencil thickness is typically dictated by other components on the PCB such as fine-pitch leaded and small discretes.

No minimum solder paste volume is typically required for PBGA since solder spheres completely melt and collapse during reflow.

Apertures same as PCB pad diameters generally provide the best gasketing. In some cases, such as larger body size PBGAs, a thicker stencil may provide improved assembly robustness.

± 0.025 mm solder paste print to PC board registration is common – paste should never touch any surrounding exposed metallization.

Round Apertures for PBGA Printing

Wet Solder Paste on PBGA PCB Pads
Surface Mount Assembly of PBGA

High and low mass components should be carefully profiled with a thermocouple in a corner and inner sphere on a fully populated profile PCB. Most PBGA qualified to a maximum reflow temperature of 220°C for SnPb and 260°C for Pb-free.

Soldering profiles are solder paste dependent so follow guidelines recommended by Solder paste vendor, but here are some guidelines that can be used:

- **SnPb soldering:**
  - Raise temperature of the joints to 100°C at between 1.5 and 3.0°C/sec
  - Peak component temperature typically between 205 and 220°C
  - Desirable dwell time above 183°C between 50 and 80 secs

- **Pb-free soldering:**
  - Raise temperature of the joints to 100°C at between 1.5 and 3.0°C/sec
  - Peak component temperature typically between 235 and 245°C
  - Desirable dwell time above 217°C between 50 and 80 secs

**Reference Application Note AN3300 for additional information**
Soldering Pb-Free Spheres with SnPb Paste

Soldering Pb-free spheres with SnPb solder paste is not recommended by Freescale. If it is attempted, the entire Pb-free solder joint must reflow so that it collapses and mixes with the SnPb.

<table>
<thead>
<tr>
<th>Peak Temp (°C)</th>
<th>Comment</th>
<th>Example Solder Joints*</th>
</tr>
</thead>
</table>
| 203           | - No sphere collapse  
- No alloy mixing  
- Poor assembly yield (opens)  
- Early failures in temp cycling | Reflowed SnPb Solder Paste  
SnAgCu (Pb-free) Solder Sphere |
| 210           | - Minimal sphere collapse  
- Minimal alloy mixing  
- Poor assembly yield (opens)  
- Early failures in temp cycling | |
| 217           | - Partial sphere collapse  
- Partial alloy mixing  
- 100% assembly yield on small sample  
- Consistent interconnect reliability | |
| 225           | - Complete sphere collapse  
- Complete alloy mixing  
- Consistent 100% assembly yield  
- Excellent interconnect reliability | |

*Solder joints cross-sections shown are post-thermal cycling and show some evidence of typical fracturing.*
Profiling thermocouples should preferably be placed inside a corner and center sphere – alternately can be placed inside the package.

Hole can be drilled from the top of the package or bottom of the PCB.

Hole should be filled with thermally conductive high temperature epoxy.

Thermocouple inserted through the top of hole drilled into a PBGA (left) and from the bottom of a PCB (bottom).
Avoiding BGA Secondary Reflow

Wave soldering is often required after BGA has been soldered on the board. Secondary reflow of BGA solder joints in this operation must be avoided

- The result can be open BGA solder joints
  - PBGAs are low thermal mass packages (get hot fast)
  - The large number of plated through holes transmit heat rapidly
  - When heated from bottom only, PBGAs may warp
    - Upward bowing due to expansion of the PBGA substrate
    - Fully or partially molten solder joints separate
Avoiding BGA Secondary Reflow

There are many ways to avoid secondary reflow of BGA:

• Optimize the wave solder operation (temperature, PCB contact time) to minimize heat to the BGA
• Implement a wave solder pallet to block solder from BGA area
• Block heat transfer through vias around the BGA by filling or tenting with solder mask on wave side of board
  • May not be desirable from an in circuit test standpoint since it precludes using via pads as test points
• Apply polyimide tape under BGA area
  • Undesirable hand operation
• Redesign board to eliminate the wave solder operation
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BGA Solder Joint Voiding

Voids are common in BGA solder joints after PCB assembly

- They are typically found near the package interface
- Voids are caused by entrapped flux from the solder paste volatilizing and rising in the molten solder joint due to buoyancy

Voids in X-ray

Voids in Cross-Section
BGA Solder Joint Voiding

The IPC-A-610D Standard\(^1\) (Acceptability of Electronic Assemblies) categorizes >25% BGA joint voiding as a defect. Voiding may be reduced by many factors including selecting a solder paste with a low volatile flux and using a longer dwell time below liquidus.

Some studies have shown voided joints to be just as or more reliable than non-voided joints:

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PBGA Solder Joint Voids
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Thermal Performance
Avoiding PBGA Rework

Due to high assembly yields, PBGA rework should rarely be required.

Key areas to focus on to maintain high assembly yield and avoid PBGA rework:

- **Bare board quality** - Ensure solderable pads with soldermask not encroaching onto the pads areas except the trace
- **Solder paste printing** – Avoid solder paste skips
  - Use 3D or visual paste inspection until the process is under control
- **Solder reflow process** - Carefully profile with a fully populated PCB and minimize the temperature delta between middle and corner PBGA joints
- **Electrical test** - Ensure that functional and in-circuit test programs do not falsely blame the PBGA as the cause for electrical failures

Key points when PBGA rework must be undertaken:

- The rework process goal is joint structure, quality and reliability that is at least as good as the initial assembly
- Removing and replacing a PBGA is easier than a QFP
- PBGA rework can be accomplished with off-the-shelf equipment
- The entire rework process must be carefully characterized

Re-use of reworked PBGAs after reballing is not recommended
PBGA Detailed Rework Steps

Component Removal:

• First, the entire assembly must be baked for 4 hours minimum at the highest temperature that the most heat sensitive device on the PCB assembly can withstand (typically 80 to 125°C)
  • This is to remove moisture from the PBGA so that it will not delaminate or popcorn during removal
• PBGA can typically be removed and replaced with topside heat only
• For thicker boards with many internal planes use additional localized bottomside heat
• To reduce cycle time and minimize board warpage, preheat entire board to at least 80°C or higher, as permitted by the temperature rating of the other components that may be on the board
  • To minimize the number of heat cycles the PCB experiences, this pre-heat can be the bake-out described in the first step
  • Apply localized heat to PBGA package
  • Lift package immediately with a vacuum wand or tweezers when solder is molten

Excess Solder Removal from the PCB:

• Avoid an additional heat cycle by removing the excess solder from the PCB site immediately after package lift off, while board is still hot
• Can be removed quickly by a solder vacuum tool or solder wicking braid which requires heat and pressure and usually more time
• The goal is to end up with a solderable pad while avoiding damage the PCB or pads
PBGA Detailed Rework Steps - Continued

Re-Applying Flux to the PCB
- For a PBGA with collapsing spheres, no additional solder is needed - flux only
- Flux should be compatible with production cleaning strategy and applied uniformly but sparingly
- Re-applying solder paste may increase rework yield / reliability by accounting for PCB warpage

Placement and Reflow of Replacement PBGA
- Use the rework station or offline placement equipment
- As with removal, preheating of entire PCB may be advisable
- Characterize temperatures to provide uniform heat with ramp rates similar to reflow furnace
  - Non uniform heat and fast ramp rates can cause PBGA to warp or cause non uniform collapse of solder balls

Cleaning
- If cleaning is required, use the standard production cleaning method
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PBGA Solder Joint Reliability

PBGA construction influences solder joint reliability

- For PBGA, silicon die mismatched to other package materials causes solder joint strain from differential package/PCB expansion during thermal excursions
- Solder joints under die edge usually fail first in accelerated thermal cycling

![PBGA Solder Joint Reliability Diagram](image-url)
Solder-Joint Reliability Experiments

Purpose

• Determine life of package joined to PC Board
  • Solder-joints limit the life of final assembly

Availability

• Many new packages have data
  • Not all products will have data
    – Use existing data from similar package when available

• Experimental conditions
  • Air temperature cycling (ATC)
    – Automotive/industrial: -40/125°C, 15 minute ramps and dwells
    – Telecommunications/networking/desktop: 0/100°C, 10 minute ramps and dwells
    – Other conditions sometimes used for specific customer requirements

• Daisy chain package and boards
  – Allow resistance to be monitored during cycling to detect failures

• Other Mechanical Tests
  • Monotonic Bend, IPC-9702, limited availability
  • JEDEC Shock, JESD22-B111, limited availability

Ask your customer sales representative for experimental data.
PBGA Solder Joint Reliability

Air temperature cycling is commonly performed on mounted PBGAs to assess solder joint integrity and suitability for intended applications

- Two common conditions are 0 to 100°C (networking, telecomm, computing) and -40 to 125°C (industrial, automotive)
- Testing typically continues until >50% of the packages failed to obtain the failure distribution
Example Solder-Joint Reliability Test Board

Connection points for specialized daisy chain testing

8 sites for daisy chain packages
(Design follows guidelines of IPC-9701A.)

Edge fingers for monitoring
416 TEPBGA Solder Joint Reliability

Perimeter Solder-Joints - Varied Solder-Joint Alloy

<table>
<thead>
<tr>
<th>Bta Beta r^2 n/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>2667 22.36 0.96 32/1</td>
</tr>
<tr>
<td>4243 21.4 0.844 32/1</td>
</tr>
</tbody>
</table>

27x27 mm sq., 1 mm Pitch Package

Number of Air Temperature Cycles (-40/125°C)
388 PBGA Solder-Joint Reliability

27x27 mm sq., 1 mm Pitch Package

[Graph showing solder-joint reliability with data points and trend lines for different alloys.]
PBGA Solder Joint Reliability

Fractures in PBGA solder joints can initiate and propagate during extended board-mounted thermal cycling. Typical fractures are through bulk solder (not intermetallic).

Fracture Propagating Through Bulk Solder Near the PBGA Solder Pad
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Thermal Performance
PBGA Thermal Performance

Thermal performance is reported as thermal resistances determined per the JEDEC JESD51 series of specifications. PBGA packages typically have good thermal connection to the printed circuit board. Their performance will depend on the board construction, the thermal connection to the power and ground planes in the board, and other local heat sources. To highlight the effect of the local environment, thermal resistances are typically provided on both the single layer board and the 2s2p board (with two signal and two power planes). The planes are 1 oz copper. It is not unusual to see nearly a factor of two difference between the thermal resistances on the two boards.

A good summary description is JESD51-12, “Guidelines for Reporting and Using Electronics Package Thermal Information”

The next slide provides a cross reference to the various thermal resistances.
# Summary of Thermal Resistances

<table>
<thead>
<tr>
<th>Thermal Metric</th>
<th>Symbol</th>
<th>Condition</th>
<th>Usage</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction to Ambient</td>
<td>$R_{\theta JA}$</td>
<td>Single Layer Board</td>
<td>Tightly packed array of devices</td>
<td>JESD51-2, JESD51-6</td>
</tr>
<tr>
<td>Junction to Ambient</td>
<td>$R_{\theta JA}$</td>
<td>Four layer board (2s2p)</td>
<td>Most commonly quoted thermal resistance</td>
<td>JESD51-2, JESD51-6</td>
</tr>
<tr>
<td>Junction to Board</td>
<td>$R_{\theta JB}$</td>
<td></td>
<td>Customer use in modeling or when board temperature known</td>
<td>JESD51-8</td>
</tr>
<tr>
<td>Junction to Case</td>
<td>$R_{\theta JC}$</td>
<td></td>
<td>Heat sinks</td>
<td>MIL-SPEC883, Method 1012</td>
</tr>
<tr>
<td>Junction to Package Top</td>
<td>$\Psi_{JT}$</td>
<td>Natural Convection</td>
<td>Determine junction temperature from thermocouple reading</td>
<td>JESD51-2</td>
</tr>
</tbody>
</table>

Note: PBGA packages are tested on a board specified in JESD51-9

Jedec JESD specs are available at www.jedec.org
Typical PBGA Power Capabilities

\[ R_{\theta JA} = \frac{T_J - T_A}{P} \implies P = \frac{T_J - T_A}{R_{\theta JA}} \]

**Assumptions:** Multilayer application, lots of board area, only low power devices nearby, used junction to ambient thermal resistance on 2s2p test board in natural convection with maximum junction temperature 35 C higher than ambient temperature. Range in thermal performance caused by die size and substrate design features.
# Thermal Data for Three Package Configurations

<table>
<thead>
<tr>
<th>Thermal Metric</th>
<th>Test Board</th>
<th>Symbol</th>
<th>PBGA $\theta_JA$</th>
<th>TEPBGA $\theta_JA$</th>
<th>TEPBGA2 $\theta_JA$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction to Ambient</td>
<td>Single layer board (1s)</td>
<td>$\theta_JA$</td>
<td>57</td>
<td>31</td>
<td>25</td>
<td>°C/W</td>
</tr>
<tr>
<td>Natural Convection</td>
<td>Four layer board (2s2p)</td>
<td>$\theta_JA$</td>
<td>28</td>
<td>21</td>
<td>17</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction to Ambient (200 ft/min)</td>
<td>Single layer board (1s)</td>
<td>$\theta_JMA$</td>
<td>49</td>
<td>25</td>
<td>19</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction to Ambient (200 ft/min)</td>
<td>Four layer board (2s2p)</td>
<td>$\theta_JMA$</td>
<td>25</td>
<td>18</td>
<td>14</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction to Board</td>
<td></td>
<td>$\theta_JB$</td>
<td>21</td>
<td>13</td>
<td>9</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction to Case</td>
<td></td>
<td>$\theta_JC$</td>
<td>13</td>
<td>9</td>
<td>7</td>
<td>°C/W</td>
</tr>
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<td>Junction to Package Top</td>
<td>Natural Convection</td>
<td>$\psi_{JT}$</td>
<td>3</td>
<td>2</td>
<td>7</td>
<td>°C/W</td>
</tr>
</tbody>
</table>
Effect of Die Size

Thermal performance depends on package construction, package internal design, and die size. Theta-JC decreased 30% as die area increased by 75% for this 416 27x27 mm TEPBGA2.

![Graph showing the effect of die size on thermal performance](image-url)
Summary: PBGA Thermal Performance

Thermal performance is typically available in the Data Sheets for the product.

- For Networking products, it is in the “hardware specification,” for other products it will be in the product manual or datasheet. Data is usually in the “electrical specifications” section of the manual if there is not a separate thermal section.
- Thermal performance depends on die size and package design. Data should be obtained specific to the device.

Thermal performance is determined per the JESD51 series of specifications with the PBGA mounted to a board. A good summary description is JESD51-12, “Guidelines for Reporting and Using Electronics Package Thermal Information”. These specifications are available at [http://www.jedec.org](http://www.jedec.org).

Temperature predictions using $R_{\theta JA}$ have potential errors of 2X because of uncertainty in ambient conditions and effect of other power sources.