Errata to G2 PowerPC™ Core Reference Manual, Rev 0

The G2 core is an implementation of the PowerPC™ microprocessor family. This errata describes corrections to the G2 PowerPC Core Reference Manual, Rev. 0. For convenience, errata items refer to the section and page numbers in the reference manual. The section and page numbers that appear in bold have been added since the last revision of this document.

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xxv Under the heading ‘Organization,’ in the first bullet, replace the statement in parenthesis in the second sentence with the following:

(including instruction and data cache way-locking for the G2 core)

1.3.3.3, 1-26 Cache way-locking is a feature of both the G2 core and the G2_LE. Remove ‘G2_LE-Only’ from the heading and replace the paragraph with the following:

The G2 core implements instruction and data cache way-locking, which guarantees that certain memory accesses will hit in the cache. This provides deterministic access times for those accesses. See Chapter 4, “Instruction and Data Cache Operation,” for more information.

1.4, 1-40 In Table 1-6, “Differences Between G2 and G2_LE Cores,” replace the rows on cache locking with the following:
2.1.2.1, 2-11 In Table 2-5, “HID0 Bit Functions,” remove “do not clear.” from the description of bit 1 and replace the row with the following:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

2.1.2.3, 2-14 Replace the first sentence of the first paragraph with the following:
The G2 core implements an additional hardware implementation-dependent HID2 register, shown in Figure 2-4, which enables cache way-locking; the G2_LE core also enables true little-endian mode and the new additional BAT registers.

Chapter 4, 4-1 Replace the last sentence of the second paragraph with the following:
It also describes the cache way-locking features provided in the G2 core.

4.2.3.3, 4-5 Replace the second paragraph with the following:
Note that the G2 core also provides instruction cache way-locking in addition to entire instruction cache locking as described in Section 4.12, “Cache Locking.”

4.3.3.3, 4-7 Replace the second paragraph with the following:
Note that the G2 core also provides instruction cache way-locking in addition to entire data cache locking as described in Section 4.12, “Cache Locking.”

4.5.2, 4-10 In Figure 4-3, “Double-Word Address Ordering—Critical-Double-Word-First,” remove ‘G2_LE Core Cache Address’ from the first heading and replace it with the ‘G2 Core Cache Address.’

4.12, 4-32 Replace the first paragraph with the following:
This section describes the entire cache locking and cache way-locking features of the G2 core.

4.12.1, 4-32 The title of the second bullet should be: ‘Way-Locking.’

4.12.2, 4-33 The title of Table 4-11 should read, “HID2 Bits Used to Perform Cache Way-Locking.”

4.12.3.1, 4-34 Replace the first paragraph with the following:
This section describes the procedures for performing data cache locking on the G2 core.
4.12.3.1.3, 4-35 In Table 4-14, “MSR Bits for Disabling Exceptions,” replace the description of bit 24 with the following:

<table>
<thead>
<tr>
<th>24</th>
<th>CE</th>
<th>Critical interrupt enable</th>
</tr>
</thead>
</table>

4.12.3.1.7, 4-37 Replace the first paragraph with the following:

Data cache way-locking is controlled by HID2[DWLCK], bits 24–26. Table 4-15 shows the HID2[DWLCK 0–2] settings for the G2 core embedded processor.

4.12.3.1.7, 4-37 The title of Table 4-15 should read, “G2 Core DWLCK[0–2] Encodings.” Replace the paragraph after Table 4-15 with the following:

The following assembly code locks way 0 of the G2 core data cache:

4.12.3.2, 4-38 Replace the first paragraph with the following:

This section describes the procedures for performing instruction cache locking on the G2 core.

4.12.3.2.3, 4-40 In Table 4-17, “MSR Bits for Disabling Exceptions,” replace the description of bit 24 with the following:

<table>
<thead>
<tr>
<th>24</th>
<th>CE</th>
<th>Critical interrupt enable</th>
</tr>
</thead>
</table>

4.12.3.2.6, 4-42 Remove ‘(G2_LE Only)’ from the heading and replace the first paragraph with the following:

Instruction cache way-locking is controlled by the HID2[IWLCK], bits 16–18. Table 4-18 shows the HID2[IWLCK 0–2] settings for the G2 core embedded processor.

4.12.3.2.6, 4-42 The title of Table 4-18 should read, “G2 Core IWLCK[0–2] Encodings.” Replace the paragraph after Table 4-18 with the following:

The following assembly code locks way 0 of the G2 core instruction cache:

4.12.3.2.6, 4-42 Replace the last paragraph with the following:

In the second method, the instruction cache block invalidate (icbi) instruction can be used to invalidate individual cache blocks. The icbi instruction invalidates blocks in an entirely locked instruction cache. The icbi instruction also may invalidate way-locked blocks within the instruction cache.

6.5.2.2.2, 4-43 Replace the third line “bdnzf, 0, im1” of function “im1” with “bdnzf, eq, im1”

Replace the fourteenth line “srw, r1, r1, 8” of function “im1” with “srwi, r1, r1, 8”

8.3.15.3, 8-55 Remove the second sentence from the timing comments of “PLL Configuration (core_pll_cfg[0:4])—Input”

These bits may be read through HID1[PC0–PC4].
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