1 Purpose

This document provides guidelines for handling and assembly of NXP PQFN packages during Printed Circuit Board (PCB) assembly. Guidelines for PCB design, rework, and package performance information such as Moisture Sensitivity Level (MSL) rating, board level reliability, and mechanical and thermal resistance data are included for reference.

2 Scope

This application note contains generic information encompassing various NXP PQFN packages assembled internally or at external subcontractors. It should be noted that the specific information about each device is not provided. This document serves only as a guideline to help users develop a specific solution. Actual experience and development efforts are still required to optimize the assembly process and application design per individual device requirements, industry standards such as IPC and JEDEC, and prevalent practices in user's assembly environment.

For assistance for more details or questions about the specific devices contained in this note, visit www.nxp.com or contact the appropriate product application team.
3  Power quad flat no-lead (PQFN) package

3.1  Package description

The PQFN is a surface mount plastic package with lead pads located on the bottom surface of the package. All PQFN packages have either been designed with a single exposed die pad or multiple exposed die pads, depending on device requirements and intended application. The industry standardization committee, JEDEC, has given a registered designator of MO-251 to describe the family of single exposed pad PQFN packages.

![Figure 1. PQFN standard (left) and PQFN custom (middle/right) packages from NXP](image)

3.2  Package dimensioning

PQFN packages range from 5.0 mm x 5.0 mm to 12 mm x 12 mm in body size with 2.1 mm height. Lead counts range from 16 to 36. The lead pads have been designed in single-row configurations only. The lead pitch of the perimeter leads is available in 0.80 mm and 0.9 mm designs, as shown in Table 1. PCB layout and stencil designs are critical to ensure sufficient solder coverage between the package and the printed circuit board (PCB). When designing the PCB layout, refer to the NXP case outline drawing to obtain the package dimensions and tolerances.

Table 1. NXP PQFN package dimensions

<table>
<thead>
<tr>
<th>Bottom view</th>
<th>Package</th>
<th>Body size (mm)</th>
<th>Lead pitch (mm)</th>
<th>IO count</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PQFN 16</td>
<td>5.0 x 5.0 x 2.1</td>
<td>0.8</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td>PQFN 32</td>
<td>8.0 x 8.0 x 2.1</td>
<td>0.8</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td>PQFN 36</td>
<td>9.0 x 9.0 x 2.1</td>
<td>0.8</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>PQFN 16</td>
<td>12 x 12 x 2.1</td>
<td>0.9</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td>PQFN 23</td>
<td>12 x 12 x 2.1</td>
<td>0.9</td>
<td>23</td>
</tr>
<tr>
<td></td>
<td>PQFN 24</td>
<td>12 x 12 x 2.1</td>
<td>0.9</td>
<td>24</td>
</tr>
<tr>
<td></td>
<td>PQFN 36</td>
<td>12 x 12 x 2.1</td>
<td>0.8</td>
<td>36</td>
</tr>
</tbody>
</table>

Part interchangeability is a concern when primary and secondary suppliers both provide production parts. Additional information of this topic is provided in Printed circuit board guidelines, page 5.
3.3 Package design

3.3.1 Cross section

A typical PQFN cross section, depicted in Figure 2, illustrates a lead frame based package with wirebonding technology. The die is usually soldered to NiPdAu pre-plated thick copper leadframe with die pad (or flag) exposed external to the package. Either gold, copper, or combination of gold, copper, and heavy gauge aluminum wire are used for wire bonding between die to lead and die to die. NXP PQFN design is a molded array package (MAP), which uses a sawn singulation process.

![Figure 2. Cross-section of a custom PQFN MAP (molded array package)](image)

3.3.2 Lead terminal types

NXP offers two different lead terminal types: "E" and "S" style, for PQFN packages.

3.3.2.1 PQFN: "E" type

The E-type lead frames are half etched from the top, where the lead posts are exposed all the way to the edge of the package (viewed from the bottom of the package, see left photo in Figure 3). The "E" version follows JEDEC MO-220 (PQFN) design guidelines. The lead extends to the package perimeter, where the lead ends are fully exposed to the side of the package. A solder fillet is expected to form and should be visible on the PCB after the solder reflow process. However, a solder fillet is not guaranteed and is dependent upon the board and stencil design, solder paste flux composition, solder paste volume, and assembly process conditions. Following the guidelines in PCB pad design, page 8 ensures optimal results. E-type lead frames are considered standard NXP design.

![Figure 3. MAP PQFN "E" version: left-bottom view, right-tilted to show side and bottom views](image)
3.3.2.2 PQFN: "S" type

The "S" style is a NXP version based on JEDEC MO-220, with an exception in the lead end feature. The S-type lead frames (see right photo in Figure 4) are half etch from the bottom where there is mold compound between the edge of the lead post to the edge of the package. The lead end is slightly recessed from the package perimeter due to a half-etched lead frame. No solder fillet is expected after the solder reflow process. The S-type was the original PQFN design, and NXP still supports S-type lead frames in production. All new products moving forward use the E-type lead frames.

Figure 4. PQFN "S" version: left - bottom view; right - tilted to show side and bottom views
4 Printed circuit board guidelines

4.1 PCB design guidelines and requirements

As the package size shrinks and the lead count increases, the dimensional tolerance and positioning accuracy affects subsequent processes. Part interchangeability is also a concern when two separate suppliers provide production parts for the PCB. The optimized PCB layout for one supplier may have issues (manufacturing yield and/or solder joint life) with the other supplier’s parts. When more than one source is expected, the PCB layout should be optimized for both parts.

A proper PCB footprint and stencil designs are critical to surface mount assembly yields and subsequent electrical and mechanical performance of the mounted package. The design starts with obtaining the correct package drawing. Package case outline drawings are available at www.nxp.com. Follow the procedures in Case outline drawing, MCDS, and MSL information download, page 31.

NXP provides extended case outline data including PCB design guidelines for Cu, solder mask, and solder stencil design, for a variety of packages. Check the package case outline document first for such information. If available, it is recommended to use the guidelines of the case outline as a baseline to create a user specific solution of the PCB design.

An example of an extended case outline drawing for 12 mm x 12 mm PQFN is shown in Figure 5 and Figure 6. The goal is a well soldered PQFN pad as is shown in Figure 7.
Figure 5. Example of 12 mm x 12 mm 16 lead PQFN extended case outline drawing (part 1)
Figure 6. Example of 12 mm x 12 mm 16 lead PQFN extended case outline drawing (part 2)

Figure 7. Example of a well soldered PQFN package pad on a robust pad design. The image shows an E-style PQFN package.
4.2 PCB pad design

4.2.1 General pad guidelines

NXP follows the Generic Requirements for Surface Mount Design and Land Pattern Standards from the Institute for Printed Circuits (IPC), IPC-7351B. The document and an accompanying land pattern calculator can be purchased from the IPC's web site landpatterns.ipc.org, and includes guidelines for a large number of PQFN's, based on assumed package dimensions. NXP also recommends considering the guidelines given IPC-7093 (Design and Assembly Process Implementation for Bottom Termination Components) for QFN PCB and process design.

Some general guidelines for perimeter pads on PQFN footprints are:

- All PCB pad calculations should be based on the nominal size of the package pad.
- Perimeter PCB Cu pad length under the package should be the nominal value for the length.
- PCB Cu pad lengths exterior to the package edge should be at least 0.2 mm long, for standard designs.
- PCB Cu pad lengths exterior to the package edge should be at least 0.4 mm long, for customers seeking the inspectable solder joint packages to form an inspectable solder joint.

![Figure 8. Standard pad length and recommended pad length for inspectable solder joints](image)

- PCB Cu pad lengths exterior to the package edge should be at least 0.4 mm long, for customers seeking the inspectable solder joint packages to form an inspectable solder joint.

- Perimeter PCB Cu pad width should be approximately:
  - For a lead pitch < 0.8 mm: Add 12.5 µm on each side to the nominal lead width (i.e. 0.525 mm wide PCB Cu pad for a 0.5 mm nominal lead width)
  - For a lead pitch ≥ 0.8 mm: Add 25 µm on each side to the nominal lead width (i.e. 0.85 mm wide PCB Cu pad for a 0.8 mm nominal lead width)

- Pitch needs to be designed in metric using the exact dimensions of 0.65 mm, 0.80 mm, and 0.9 mm
- No insertion (THT---Through Hole Technology) components or PCB vias should be placed at a distance less than 2.0 mm from the package land area.
- For perimeter PCB pads, it is recommended to use NSMD (Non Solder Mask Defined), as they provide significant advantages over SMD (Solder Mask Defined) pads, in terms of dimensional tolerances and registration accuracy. The NSMD has a solder mask opening larger than the copper pad, and the PCB pad area is controlled by the size of the copper pad. Since the copper pad etching process is rather capable and stable, a smaller size copper pad can be defined more accurately. The clearance around the copper pad and solder mask should be at least 75 µm, to account for the registration tolerance of the solder mask. See Figure 9 on pad design concept.

![Figure 9. NSMD pad design](image)
4.2.2 Thermal/electrical pad guidelines

PQFN packages are thermally/electrically enhanced leadframe technology based, and the bottom of the package provides the primary heat removal path, as well as excellent electrical grounding to the PCB through an exposed pad (EP). In a PQFN package, the die attach paddle is at the same level as the perimeter pads within the package such that the pad is exposed during the mold process, as shown in Figure 10. Orange arrows here stand for heat flow. To optimize thermal performance, the PCB design should include a thermal copper plane, as shown in Figure 10.

![Figure 10. Cross-section of PQFN-EP package with heat transfer schematic](image)

Although the land pattern design of the perimeter pads for exposed pad attachment on the PCB should be the same as that for conventional, non-thermally/electrically enhanced packages, extra features are required during the PCB design and assembly stage for effectively mounting thermally/electrically enhanced packages. In addition, repair and rework of assembled packages may involve some extra steps, depending upon the current rework practice within the company.

4.2.3 Exposed pad design, spacing between PCB perimeter pads and EP for PQFN packages with symmetric perimeter pad design and central single exposed pad

![Figure 11. Example of PQFN package with symmetric perimeter pad and single exposed pad](image)

The design of the land pattern and the size of the thermal pad depend strongly on the thermal characteristics and power dissipation of the specific product and application. To maximize both removal of heat from the package and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad as shown in Figure 12. The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package. However, the solderable area, which should be defined by the solder mask, should be approximately the same size/shape as the exposed pad area on the package, to maximize the thermal/electrical performance. A clearance of at least 0.25 mm should be designed on the PCB between the outer edges of the exposed pad land pattern and the inner edges of perimeter pad pattern to avoid any shorts. This topic is discussed in more detail in Solder stencil/solder paste, page 18.
4.2.3.1 Alternative exposed pad design

Alternatively, the exposed pad solder land can be segmented into a symmetric pad array as shown below in Figure 13. The pad array can be created either by segmentation of a full copper area by solder mask, or copper defined outlines using NSDM defined pads. Recommended edge length of a matrix pad is between 1.0 mm to 2.0 mm, the distance between the pads should be 0.4 mm.

The segmented PCB design facilitates the solder paste flux outgassing during reflow, thereby promoting a lower voiding level of the completed solder joint. At the same time, the maximum size of a single solder void is limited by the dimensions of a single matrix segment.

4.2.3.2 Vias in the PCB exposed pad land pattern

While the land pattern on the PCB provides a means of heat transfer/electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). These vias act as “heat pipes”. The number of vias is application specific and dependent upon the package power dissipation, as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number required. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern with a 1.2 mm grid, as shown in Figure 14.
It is also recommended the via diameter should be 0.30 mm to 0.33 mm with 1.0 oz. copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process, which may result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be also filled or "tented" with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 0.1 mm (4.0 mils) larger than the via diameter.

Note: These recommendations are to be used as a guideline only.

Figure 14. PCB exposed pad land pattern via grid

4.2.4 Exposed pad design, for PQFN packages with non-symmetric perimeter pad design and multiple exposed pads

The design of the land pattern and the size of the thermal pad depend strongly on the thermal characteristics and power dissipation of the specific product and application. To maximize both removal of heat from the package and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad as shown in Figure 15. The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package.

Some general guidelines for perimeter pad on PQFN exposed pad footprints are:

- All PCB exposed pad calculation should be based on the nominal size of the package exposed pad size
- The size of the PCB exposed pad land pattern should be approximately the same as the nominal size of the corresponding package exposed pad.
- Making the PCB pad 1:1 shape may not be valuable. Instead, the PCB pad should be "square" to the package pad side. See Figure 16 for example.
- The PCB Cu pad lengths should extend from the package edge by 0.2 mm, for exposed package pads extending to the package edge (such as pad #15 and #16 in Figure 16).
- A clearance of at least 0.25 mm should be designed on the PCB between the outer edges of the exposed pad land pattern and the inner edges of perimeter pad pattern, as well as between the edges of neighbouring exposed land patterns to avoid any shorts.
If the guidelines described previously lead to unacceptably high voiding levels in board attach soldering, or prevention of high voiding levels is desired, the exposed pad PCB land pattern design can be modified as described in the following:

### 4.2.4.1 Alternative exposed pad design - option 1

The exposed pad solder land can be segmented into a pad array as shown in Figure 17. The pad array should be created by segmentation of a full copper area by solder mask webbing. Recommended edge length of a matrix pad is between 1.0 mm to 2.0 mm, the distance between the individual pads should be 0.2 mm to 0.4 mm. The minimum distance (width of the solder mask webbing) needs to be aligned with the PCB manufacturer's design rules and manufacturing capabilities. The segmented PCB design facilitates the solder paste flux outgassing during reflow, thereby promoting a lower voiding level of the completed solder joint. At the same time, the maximum size of a single solder void is limited by the dimensions of a single matrix segment.
4.2.4.2 Alternative exposed pad design option 2

Alternatively, the exposed pad solder land can be split up into a pad array of single Cu pads as shown in Figure 18. Recommended edge length of a matrix pad is between 1.0 mm to 2.0 mm, the distance between the pads should be between 0.2 mm to 0.4 mm. The segmented PCB design facilitates the solder paste flux outgassing during reflow, thereby promoting a lower voiding level of the completed solder joint. At the same time, the maximum size of a single solder void is limited by the dimensions of a single matrix segment.

4.2.4.3 Vias in the PCB exposed pad land pattern

While the land pattern on the PCB provides a means of heat transfer/electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). These vias act as "heat pipes". The number of vias is application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number required. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern at 1.2 mm grid, as shown in Figure 19.

Note: These recommendations are to be used as a guideline only.
4.2.4.4 Vias in alternative exposed pad design - option 1

For this solder mask defined array pad design option, there are various thermal via arrangements possible.

- Via is placed in the center of the pad, as show in Figure 20 on the left image. Vias are placed in the cross-points of the solder mask webbing, as shown in Figure 20 on the right image.

All the vias in these two cases must be plugged, tented, or plated.
4.2.4.5 Vias in alternative exposed pad design - option 2

For copper defined array pad design option, it is recommended to place the thermal via in the center of the pad, as shown in Figure 21. The via must be plugged, tented, or plated.

The typical appearance of a completed exposed pad solder joint using copper defined pad array and plugged via technology is shown in Figure 22. Fully wetted PCB pad, void free solder joints with plugged, and non-wetted via area in center of each pad can be observed as expected. A cross-section of a device using similar design is shown in Figure 23.
4.2.5 Pad surface finishes

Almost all PCB finishes are compatible with PQFNs, including Hot Air Solder Leveled (HASL), Organic Solderability Protectant (OSP), Electroless Nickel Immersion Gold (ENIG), Immersion Sn, and Immersion Ag.

4.2.6 Solder mask opening for PCB area

The general solder mask guidelines for perimeter pads are discussed in General pad guidelines, page 8. Usually solder masks should be pulled away from the perimeter pads. The solder mask opening around the PCB pads can be as large as the spacing between pads. The area in between the pads may be too thin for the solder mask, resulting in the solder mask lifting off from the PCB. In general, solder mask width should be a minimum of 0.10 mm as shown in Figure 24, but this is only possible for larger pitches. If less than 0.10 mm, there may be solder mask adhesion problems. A potential solution is modification of the solder mask along the pad-to-pad spacing so only the "toes" of the pads are covered with solder mask, for better PCB strength.

![Figure 24. Pad and solder mask with thin webbing](image)

4.2.6.1 Exposed pad design, for PQFN packages with non-symmetric perimeter pad design and multiple exposed pads

The general solder mask guidelines for perimeter pads are discussed in General pad guidelines, page 8.

- It is recommended to design for solder mask pull-back from the copper pad edge for the PCB exposed pad land pattern. The clearance between the copper pad and solder mask should be at least 0.15 mm. See Figure 25 on the solder mask design concept.
- Alternatively, the solder mask opening can be as large as the package outline, with 0.35 mm clearance on each side between nominal package edge and solder mask. See Figure 26 on the solder mask design concept.
Figure 25. Standard PCB footprint with 0.15 mm clearance around copper pads

Figure 26. Standard PCB footprint with 0.35 mm clearance between solder mask and package outline
5  Board assembly

5.1  Assembly process flow

A typical Surface Mount Technology (SMT) process flow is depicted in the SMT Process Flow in Figure 5.1.

![Figure 27. SMT process flow](image)

5.2  Solder stencil/solder paste

For maximum thermal/electrical performance, it is required for the exposed pad on the package be soldered to the land pattern on the PCB. This can be achieved by applying solder paste on both the pattern for lead attachment as well as on the land pattern for the exposed pad.

5.2.1  Solder stencil design for PQFN packages with symmetric perimeter pad design and central single exposed pad

Some general guidelines for solder stencil design on PQFN footprints are:

- All solder stencil design should be based on the nominal size of the corresponding PCB Cu pad,respectively on the nominal size of the wettable area of the corresponding PCB pad.
- Solder paste stencil aperture openings should be one-to-one (1:1) with the perimeter PCB pad sizes.
- Exposed pad stencil aperture openings should be 0.25 mm smaller than the copper pads on PCB, as shown in Figure 28. This allows for proper registration of the stencil to the pad pattern.

![Figure 28. Reduced solder stencil aperture for exposed pad](image)
A large stencil opening may result in poor release. Additionally, during the solder screen print operation, a stencil blade can both deposit solder paste, and remove, or “scoop” it out, in the large aperture openings. In the large openings, the blade bends down into the opening thereby leaving less solder volume than anticipated. To mitigate the effect of scooping, the aperture should be broken up into an array of smaller openings, i.e. by subdividing the aperture opening into an array of smaller openings, similar to the pattern shown in Figure 29.

The array of openings resemble a "window pane" pattern, as seen in Figure 29. Large PCB exposed pads are approximately 3.2 mm x 3.2 mm or larger in size should have a "window pane" stencil opening pattern. It is suggested that a spacing of 0.25 mm is used between the individual panes.

The stencil opening should be approximately 50 % to 80 % of the total PCB thermal pad area. This stencil-PCB thermal pad ratio ensures proper coverage of the thermal pad area with fewer voids and minimizes the possibility of overflow bridging to the adjacent lead.

![Figure 29. Example of window pane pattern for exposed pad stencil opening](image)

### 5.2.2 Solder stencil design for PQFN packages with non-symmetric perimeter pad design and multiple exposed pads

**5.2.2.1 Example of solder paste stencil design**

Figure 30 shows an example of solder paste stencil design on a 12x12 mm 16 PQFN PCB footprint.
5.2.2.2 Solder stencil design for perimeter I/O pads

Some general guidelines for perimeter pad solder stencil design on PQFN footprints are:

- All solder stencil design should be based on the nominal size of the corresponding PCB Cu pad, respectively on the nominal size of the wettability area of the corresponding PCB pad.
- The stencil opening should have a pullback of 0.025 mm in width on each side from the PCB Cu pad edge.
- The stencil opening should have a pullback of 0.050 mm in length on each side from the PCB Cu pad edge.
- In Figure 31 shows 1.9 mm x 0.75 mm stencil aperture opening on a 2.0 mm x 0.8 mm PCB pad.
5.2.2.3  Solder stencil design for exposed pads

Some general guidelines for exposed pads on PQFN footprints are:

- All solder stencil designs should be based on the nominal size of the corresponding PCB Cu pad, respectively on the nominal size of the wettable area of the corresponding PCB pad.

- A large stencil opening may result in poor release. Additionally, during the solder screen print operation, a stencil blade can both deposit solder paste, and remove, or “scoop” it out, in the large aperture openings. In the large openings, the blade bends down into the opening thereby leaving less solder volume than anticipated. To mitigate the effect of scooping, the aperture should be broken up into an array of smaller openings, i.e. by subdividing the aperture opening into an array of smaller openings, similar to the pattern shown in Figure 32.

- The stencil opening should have a pullback of ~0.150 mm to 0.250 mm on each side from the PCB Cu pad edge.

- The distance/spacing between the individual array stencil openings should be at least 0.250 mm, as shown in Figure 32.

- The stencil opening should be approximately 55 % to 70 % of the total PCB thermal pad area. This stencil-PCB thermal pad ratio ensures proper coverage of the thermal pad area with fewer voids and minimizes the possibility of overflow bridging to the adjacent lead.

![Figure 32. Examples of solder paste stencil design on exposed pad](image)

5.2.3  Stencil thickness

Stencil thickness can play an important role in solder joining. The stencil thickness is usually chosen by a combination of both typical industry practices and the requirements of the other components on a PCB module. NXP has had success with solder joining processing by using stencil thickness of both 0.125 mm and 0.150 mm (5.0 mils and 6.0 mils). If stencils with a thickness greater than 0.150 mm are used, it is suggested to investigate a reduction of the stencil opening size, thereby reducing total solder volume to minimize the risk of solder bridging. For stencils thinner than 0.125 mm, aperture openings may have to be increased to provide enough volume of solder to get complete solder wetting between all contact surfaces.

NXP encourages customers of PQFN packages to use stainless steel foil for the stencil material. The stainless steel stencil has a long usage life. Additionally, using a laser to cut the openings produces good opening uniformity. When followed by an electro-polish, the solder paste releases from the opening sidewalls more consistently after the printing process. Customers are strongly encouraged to use X-ray analysis before and after reflow to confirm any stencil design can provide sufficient solder paste to the PCB and also keep good separation between regions of solder paste.
5.2.4 Solder paste properties

Solder paste is one of the most important materials in the SMT assembly process. It is a homogenous mixture of metal alloy, flux, and viscosity modifiers. The metal alloy particles are made in specific size and shape. Flux has a direct effect on soldering and cleaning, and it is used to precondition the surfaces for soldering by removing minor surface contamination and oxidation. There are two different flux systems commonly available. The first type requires cleaning such as standard rosin chemistries and water soluble chemistries. Standard rosin chemistries are normally cleaned with solvents, semi-aqueous solutions or aqueous/saponifier solutions while the water soluble chemistries are cleaned with pure water. The second flux system type requires no cleaning, but normally a little residue remains on the PCB after soldering. In general, it is recommended to use a no-clean solder paste, as cleaning of flux residues from underneath the package is not feasible for PQFN package due to the low package stand-off. However, the end user should evaluate their entire process and use to ensure desired results.

The spread of solder paste during reflow partially depends upon the solder paste alloy. SnPb solder alloys spread significantly better than the many lead-free pastes (i.e., SnAgCu, SnAgBiCu, etc.), given the same reflow temperature.

5.3 Component placement

The high package pad interconnection and insertion density suggests precise and accurate placement machines are preferred. To meet this tight requirement, the placement machine should be equipped with optical recognition systems, i.e., vision system, for the centering of the PCB, as well as the components during the pick and place motion. A placement accuracy study is recommended to calculate compensations required. NXP follows EIA-481-D standard for tape and reel orientation, pin 1 at top right or quadrant #2, as is shown in Figure 33. The identification of pin 1 on the bottom side of the PQFN package varies from packages, and the details can be found in 98A Case outline Drawings.

![Figure 33. PQFN orientation in tape and reel](image)

5.4 Soldering

A typical profile band is shown in Figure 34. The actual profile parameters depend upon the solder paste used and recommendations from paste manufacturers should be followed. Temperature profile is the most important control in reflow soldering and it must be fine tuned to establish a robust process. In most cases, thermocouples should be placed under the heaviest thermal mass device on the PCB to monitor the reflow profile. Generally, when the heaviest thermal mass device reaches reflow temperatures, all other components on the PCB acquire the reflow temperature as well. Nitrogen reflow is recommended to improve solderability and to reduce defects such as solder balls.

![Figure 34. General solder reflow phases](image)

It is also recommended to monitor the temperature profile of package top surfaces to validate the package peak temperature does not exceed MSL classification of individual devices.
The solder paste needs to be taken into account for the reflow profile for all devices on the PCB. Every paste has a flux, and the flux dominates the reflow profile for steps like soak time, soak temperature, and ramp rates. Peak reflow temperature is the melting temperature of the metals in the paste, plus a "safety" margin to ensure all solder paste on the PCB reflows. The reflow profile for exposed pad packages need not be any different than the one used for non-thermally/electrically enhanced packages.

The reflow profile should follow the paste supplier's "recommended" profile. Deviation from the recommended profile should be evaluated first using a copper (Cu) coupon test. The horizontal size for a typical solder paste volume is measured as either a diameter or as "x" and "y" lengths. The Cu coupon is then reflowed and the solder paste volume is measured for either diameter or "x" and "y". The goal is to have a reflow profile with the most horizontal spread. For best results, the Cu coupon should be lightly sanded before use to remove Cu-oxide build up.

### 5.5 Inspection

Unlike traditional leaded components, the solder joints of PQFN are formed primarily underneath the package. Optical inspection and x-ray inspection are recommended to verify any open or short-circuits (bridging) after reflow. Micro-sectioning is another method of inspecting solder joint quality during process optimizations, but is less suitable to production inspection due to slow processing. Figure 5.5 shows the expected x-ray image of a soldered component. The voids under the paddle are not regarded as defective.

![Figure 35. X-ray image of assembled 44 PQFN 9x9 with segmented exposed pad solder land, thermal vias in the exposed pad land and daisy chain wire bond configuration](image)

### 5.6 Common PQFN board assembly defects

![Figure 36. Image of assembled PQFN with shorts/bridging on perimeter pads](image)
6 Repair and rework procedure

6.1 Repairing
The repair of single solder joint of PQFN or the soldered exposed die pad is not recommended because the joint/pin or EP is underneath the package.

6.2 Reworking
If a defective component is observed after board assembly, the device can be removed and replaced with a new one. This rework can be performed using the heating methods described in the following section. The following items must be observed when performing the rework.

- The influence of the heating on adjacent packages must be minimized. Care should be taken to not exceed the temperature rating of the adjacent package.
- Heating conditions differ due to differences in the heat capacities of the PCB (board thickness, number of layers) and mounted components used; thus, the conditions must be set to correspond to the actual product and its mounted components.
- NXP follows industry standard component level qualification requirements which include three solder reflow passes. The three reflow passes simulate board level attach to a double sided board and includes one rework pass. The removed PQFN package should be properly disposed of so that they do not mix in with new components.

A typical PQFN rework flow process is:
1. Tooling Preparation
2. Package Removal
3. Site Redressing
4. Solder Paste Printing
5. Remount package
6. Reflow Soldering
7. Visual check

Note: NXP product quality guarantee/warranty does not apply to products which were removed, thus, component reuse should be avoided if at all possible.
In any rework, the PCB is heated. The thermal limits of PCB and components (e.g. MSL information) have to be followed. During heating, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the components and PCB. To prevent moisture induced failures, it is recommended the PCBs and components have had strict storage control with a controlled environment such as dry air or nitrogen. In addition, a prebake is recommended to remove the moisture from components and PCB prior to removal of the PQFN, if the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly. An example prebake consists of 125 °C for 24 hours for boards with SMT components, or 95 °C for 24 hours for boards with temperature sensitive components.

Individual process steps for reworking a PQFN package are as follows:

### 6.2.1 Tooling preparation

Various rework systems are available on the market - In general, the rework station should have a split light system, an XY table for alignment, and a hot air system with a top and bottom heater for component removal. For processing PQFN packages, a system should meet the following requirements:

- **Heating**: Controlled hot air transfer (temperature and air flow) to both the PQFN package and its mounted PCB is strongly recommended. The heating should be appropriate for the correct package size and thermal mass. PCB preheating from beneath is recommended. Infrared heating can be applied, especially for preheating the PCB from the underside, but it should only augment the hot air flow from the upper side (component side). Nitrogen can be used instead of air. Additional information can be found in Package removal, page 25.
- **Vision system**: The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of the package to PCB, a split light system should be implemented. Microscope magnification and resolution should be appropriate for the pitch of the device.
- **Moving and additional tools**: Placement equipment should have good accuracy. In addition, special vacuum tools may be required to remove solder residue from PCB pads.

### 6.2.2 Package removal

If a component is suspected to be defective and is returned, no further defects must be introduced to the device during removal of the component from the PCB as this may interfere with subsequent failure analysis. The following recommendations are intended to reduce the chances of damaging a component during removal:

- **Moisture removal**: Dry bake components before removal at 125 °C for 16 to 24 hours for boards with SMT components, or 95 °C for 16 to 24 hours for boards with temperature sensitive components.
- **Temperature profile**: During de-soldering, ensure the package peak temperature is not higher and temperature ramps are not steeper than the standard assembly reflow process.
- **Mechanics**: Do not apply high mechanical forces for removal. High force can damage the component and/or the PCB which may limit failure analysis of the package. For large packages, pipettes can be used (implemented on most rework systems); for small packages, tweezers may be more practical.

If suspected components are fragile, it is especially necessary to determine if they can be electrically tested directly after de-soldering, or if these components have to be preconditioned prior to testing. In this case, or if safe removal of the suspected component is not possible or too risky, the whole PCB or the part of the PCB containing the defective component should be returned.

To remove the faulty component from the board, hot air should be applied from the top and bottom heaters. An air nozzle of correct size should be used to conduct the heat to the PQFN component leads such that a vacuum pick up tool can properly remove the component. The temperature setting for the top heater and the bottom heater is dependent on the component rating. The pictorial procedure is shown in Figure 38. Many assembly sites have extensive in-house knowledge on rework, and their experts should be consulted for further guidance.
If the PCB is large, it is important to avoid bending of the printed circuit material due to thermal stress, so a bending prevention tool must be placed on the bottom of the printed circuit board, and a bottom heater installed to allow heating of the entire printed circuit board in order to raise work efficiency.

### 6.2.3 Site redressing

After the component is removed, the PCB pads have to be cleaned to remove solder residue to prepare for the new component placement. This may be completed by vacuum de-soldering, solder sucker, solder wick braid, etc. after applying flux. Remaining solder residue and projections cause the solder stencil to not closely adhere to the substrate during solder paste printing, leading to improper solder paste supply during component mount.

Moreover, when the solder residue flows all the way to an adjacent through-hole, the solder paste printed on the pad can be transferred, via suction, to the through-hole during reflow, which may cause improper connection. A solvent may be necessary to clean the PCB of flux residue. A de-soldering station can be used for solder dressing. It should be noted that the applied temperature should not exceed 245 °C, which can contribute to PCB pad peeling from the PCB. This is typically a manual operation directly attributed to experience and skill.

Non-abrasive or soft bristle brushes should be used as abrasive brushes can contribute to bad solder joints (e.g. steel brushes). Prior to placing a new component on the site, solder paste should be applied to each PCB pad by printing or dispensing. A no-clean solder paste is recommended.

### 6.2.4 Solder paste printing

Solder supply during rework is done using specialized templates and tools. A mini stencil with the same stencil thickness, aperture opening, and pattern as the normal stencil are placed in the component site. A mini metal squeegee blade deposits solder paste in the specific area. See Figure 39. The printed pad should be inspected to ensure even and sufficient solder paste before component placement.

In situations where neighboring parts are at close proximity with the PQFN components, and the mini-stencil method is not an option, apply solder paste carefully on each pad using a paste dispensing system. The volume of solder paste must be controlled in order to prevent shorting on the component and/or neighboring components.

![Figure 38. Package removal process](image)

![Figure 39. Mini stencil and mini squeegee](image)
6.2.5 Package remount

After preparing the site, the new package can be placed onto the PCB. When remounting the package, it is recommended to use rework equipment that has good optical or video vision capability. A split light system displays images of both package leads and PCB pads by superimposing two images. Alignment of the leads and pads is completed with an adjusting XY which enables correct soldering. See Figure 40.

Regular lead array PQFN exhibits self-alignment in any direction including X-axis shift, Y-axis shift, and rotational misplacement. The exposed pad may not exhibit a strong self-alignment capability and precise placement of the component on the PCB is required.

![Figure 40. Split light placement images](image)

6.2.6 Reflow soldering

The new component is soldered to the PCB using the same temperature profile as the normal reflow soldering process, shown in Soldering, page 22. During soldering, the package peak temperature and temperature ramps cannot exceed those of the standard assembly reflow process.

In IR or convection processes the temperature can vary greatly across the PC board, depending on the furnace type, size and mass of components, and the location of components on the assembly. Profiles must be carefully tested to determine the hottest and coolest points of the assembly. The hottest and coolest points should fall within recommended temperatures in the reflow profile. To monitor the process, thermocouples must be carefully attached with very small amounts of thermally conductive grease or epoxy directly to the solder joint interface between the package and board.

The materials used in rework do have a higher potential to create conductive traces /corrosion etc. compared to standard materials. The PCB might need to be cleaned if it does not clean in the “normal” process, or the rework was not done using "no clean" materials.
7 Board level reliability

7.1 Testing details

Solder Joint Reliability (SJR) testing is performed to determine a measure of board level reliability when exposed to thermal cycling. Information provided here is based on experiments executed on PQFN devices using a daisy chain bond configuration. Actual surface mount process and design optimizations are recommended to develop an application specific solution. For automotive grade product applications, NXP typically prefers to reach a minimum of 2000 cycles before first solder joint failure in SJR experiments. The widely accepted temperature range for testing is -40 °C to +125 °C. Consumer SJR temperature cycling conditions may vary widely depending on the application and specific user. Typically, NXP consumer SJR testing is performed from 0 °C to +100 °C.

Table 2 shows the NXP standard test set-up for performing board level solder joint reliability testing.

Table 2. Board level reliability setup

<table>
<thead>
<tr>
<th>PCB Board</th>
<th>Test Board Assembly</th>
</tr>
</thead>
<tbody>
<tr>
<td>• 1.58 mm thickness</td>
<td>• Pb-free solder paste SAC387</td>
</tr>
<tr>
<td>• four Cu Layer</td>
<td>• Reflow peak temperature for SAC assembly ~240 °C</td>
</tr>
<tr>
<td>• OSP surface finish</td>
<td>• Pb solder paste Sn63Pb37</td>
</tr>
<tr>
<td></td>
<td>• Reflow peak temperature for SnPb assembly ~220 °C</td>
</tr>
<tr>
<td></td>
<td>• 0.100 to 0.150 mm thickness (depending on the device pitch) Ni plated, laser cut and electro-polished stainless steel stencil</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Cycling Conditions</th>
<th>Package Test Vehicle</th>
</tr>
</thead>
<tbody>
<tr>
<td>• continuous in-situ daisy chain monitoring per IPC-9701A</td>
<td>• Production BOM package including die (die mechanically present, without wire bond connection)</td>
</tr>
<tr>
<td>• Air-temperature cycling (ATC) for Automotive</td>
<td>• Daisy chain bond pattern on lead to allow continuous monitoring</td>
</tr>
<tr>
<td>• -40 °C/125 °C</td>
<td></td>
</tr>
<tr>
<td>• 15 minute ramp/15 minute dwell</td>
<td></td>
</tr>
<tr>
<td>• 1.0 hour cycle time</td>
<td></td>
</tr>
<tr>
<td>• Air-temperature cycling (ATC) for Commercial and Industrial</td>
<td></td>
</tr>
<tr>
<td>• 0 °C/100 °C</td>
<td></td>
</tr>
<tr>
<td>• 10 minute ramp/20 minute dwell</td>
<td></td>
</tr>
<tr>
<td>• 1.0 hour cycle time</td>
<td></td>
</tr>
</tbody>
</table>

7.2 Solder joint reliability results

NXP experimentally gathers board-level reliability data for a variety of packages. Results from these experiments, including Weibull plots, may be requested by customers by contacting the NXP sales team.
8 Thermal characteristics

8.1 General thermal performance

Since the thermal performance of the package in the final application depends on a number of factors (i.e. board design, power dissipation of other components on the same board, ambient temperature), the thermal package properties provided by NXP should only serve as a guideline for the thermal application design. In applications where the thermal performance is considered to be critical, NXP recommends to run application specific thermal calculations in the design phase to confirm the on-board thermal performance.

PQFN packages require the exposed pad to be connected to the PCB for thermal and/or electrical measurement. For optimized thermal performance, it is recommended to form a thermal pass into the PCB by connecting the exposed pad to the top and/or bottom and/or inner copper layers of the PCB. The PCB copper area and number of thermal vias connected to the exposed pad required to achieve the proper thermal performance on the PCB is application specific and depends on the package power dissipation and the individual board properties (thermal resistance of the application PCB).

8.2 Package thermal characteristics

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance. Additional factors to be considered in PCB design and thermal rating of the final application amongst others are:

- Thermal resistance of the PCB (thermal conductivity of PCB traces, number of thermal vias, thermal conductivity of thermal vias)
- Quality and size of PCB solder joints (effective PCB pad size, potential solder voiding in the thermal path solder joints which may reduce the effective solder area)

The thermal characteristics of the package provide the thermal performance of the package when there are no nearby components dissipating significant amounts of heat. The stated values are meant to define the package thermal performance in a standardized environment. Thermal properties of the individual products are usually given in the NXP product datasheets, as appropriate. Product datasheets are available under www.nxp.com. More detailed thermal properties may be requested by customers.

8.3 Package thermal properties - definition

The thermal performance of PQFN packages is typically specified by definition of thermal properties such as $R_{\theta JA}$, $R_{\theta JMA}$, $R_{\theta UB}$, $R_{\theta JC}$ and $\Psi_{JT}$ (in °C/W). Thermal characterization is performed by physical measurement and running complex simulation models under the following conditions:

- Two thermal board types: Single layer board (1s) per JEDEC JESD51-3 and JESD51-5 (exposed pad packages only), four layer board (2s2p) per JEDEC JESD51-7, and JESD51-5 (exposed pad packages only)
- Four boundary conditions: Natural convection (still air) per JEDEC JESD51-2, forced convection per JEDEC JESD51-6, thermal test board on ring style cold plate method per JEDEC JESD51-8, and cold plate method per MIL SPEC-883 method 1012.1

8.3.1 $R_{\theta JA}$: theta junction-to-ambient natural convection (still air)

Junction-to-ambient thermal resistance ($\text{Theta-JA}$ or $R_{\theta JA}$ per JEDEC JESD51-2) is a one-dimensional value measuring the conduction of heat from the junction (hottest temperature on die) to the environment (ambient) near the package in still air environment. The heat generated on the die surface reaches the immediate environment along two paths: (1) convection and radiation off the exposed surface of the package, and (2) conduction into and through the test board followed by convection and radiation off the exposed board surfaces.

8.3.2 $R_{\theta JMA}$: theta junction-to-moving-air forced convection

Junction-to-Moving-Air ($\text{Theta-JMA}$ or $R_{\theta JMA}$ per JEDEC JESD51-6) is similar to $R_{\theta JMA}$, but it measures the thermal performance of the package mounted on the specified thermal test board exposed to moving air (at 200 feet/minute) environment.
**8.3.3 R\(_{\theta\text{JB}}\): theta junction-to-board**

Junction-to-board thermal resistance (Theta-JB or R\(_{\theta\text{JB}}\) per JEDEC JESD51-8) measures the horizontal spreading of heat between the junction and the board. The board temperature is measured on the top surface of the board near the package. The measurement is done using a high effective thermal conductivity four layer test board (2s2p) per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only) on a ring style cold plate. R\(_{\theta\text{JB}}\) is frequently used by customers to create thermal models considering both package and application board thermal properties.

**8.3.4 R\(_{\theta\text{JC}}\): theta junction-to-case**

Junction-to-Case thermal resistance (Theta-JC or R\(_{\theta\text{JC}}\) per MIL SPEC-883 Method 1012.1) indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method per MIL SPEC-883 Method 1012.1, with the cold plate temperature used for the case temperature. The case is defined as either the temperature at the top of the package (for non-exposed pad packages), or the temperature at the bottom of the exposed pad surface (for exposed pad packages). For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance. R\(_{\theta\text{JC}}\) can be used to estimate the thermal performance of a package when the board is adhered to a metal housing or heat sink, or when a complete thermal analysis is done.

**8.4 Package thermal properties - example**

An example of the thermal characteristics as typically shown in the NXP product data sheet is shown in Table 3. The example applies to PQFN package size 12 mm x 12 mm x 2.1 mm, ~5.0 mm x 7.5 mm exposed pad, pitch 0.9 mm, die size ~ 4.5 mm x 7.0 mm. NXP gathers all thermal data for a variety of packages. Thermal properties such as \(R_{\theta\text{JA}}, R_{\theta\text{JMA}}, R_{\theta\text{JB}}, R_{\theta\text{JC}},\) and \(\Psi_{\text{JT}}\), may be requested by customers by contacting the NXP sales team.

**Table 3. Example of the thermal characteristics of PQFN package 12 mm x 12 mm x 2.1 mm**

<table>
<thead>
<tr>
<th>Rating</th>
<th>Board type</th>
<th>Type</th>
<th>Value</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction to Ambient (Natural Convection)</td>
<td>Four layer board (2s2p)</td>
<td>(R_{\theta\text{JA}})</td>
<td>24.5</td>
<td>°C/W</td>
<td>(1) (3)</td>
</tr>
<tr>
<td>Junction to Board</td>
<td></td>
<td>(R_{\theta\text{UB}})</td>
<td>4</td>
<td>°C/W</td>
<td>(4)</td>
</tr>
<tr>
<td>Junction to Case (Bottom / exposed pad)</td>
<td></td>
<td>(R_{\theta\text{JC}}) (bottom)</td>
<td>0.13</td>
<td>°C/W</td>
<td>(5)</td>
</tr>
<tr>
<td>Junction to Case (Top)</td>
<td></td>
<td>(R_{\theta\text{JC}}) (top)</td>
<td>11.5</td>
<td>°C/W</td>
<td>(7)</td>
</tr>
<tr>
<td>Junction to Package Top</td>
<td>Natural Convection</td>
<td>(\Psi_{\text{JT}})</td>
<td>0.5</td>
<td>°C/W</td>
<td>(6)</td>
</tr>
</tbody>
</table>

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board temperature) ambient temperature air flow power dissipation of other components on the board, and the thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the exposed pad surface as measured by the cold plate method (MIL Spec-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal resistance between the die and the package top surface as measured by the cold plate method (MIL Spec-883 Method 1012.1).
9 Case outline drawing, MCDS, and MSL rating

9.1 Case outline drawing, MCDS, and MSL information download

NXP offers Packaging, Environmental, and Compliance information at www.nxp.com, both in the parametric tables and in the device information details. Enter part number in the search box and review the package information of the specific part.

The complete case outline drawing and the Material Composition Declaration Sheet (MCDS), following the IPC-1752 reporting format, can be downloaded as a PDF file. Information on product specific Moisture Sensitivity Level (MSL) is also available in the part details.

9.2 Moisture sensitivity level

The Moisture Sensitivity Level (MSL) indicates the floor life of the component, its storage conditions, and handling precautions after the original container is opened. The permissible time (from opening the moisture barrier bag until the final soldering process) a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity.

In many cases, moisture absorption leads to moisture concentrations in the component high enough to damage the package during the reflow process. The expansion of trapped moisture can result in interfacial separation, known as delamination, of the mold compound from the die or lead-frame, wire bond damage, die damage, and internal cracks. In the most severe cases, the component bulges and pops, known as the "popcorn" effect.

Thus it is necessary to dry moisture-sensitive components, seal them in a moisture barrier antistatic bag with a desiccant and a moisture indicator card, which is vacuum sealed according to IPC/JEDEC J-STD-033, and only remove them immediately prior to assembly to the PCB.

*Table 4* presents the MSL definitions per IPC/JEDEC's J-STD-20. Please refer to the "Moisture Sensitivity Caution Label" on the packing material, which contains information about the moisture sensitivity level of NXP products. Components must be mounted and reflowed within the allowable period of time (floor life out of the bag), and the maximum reflow temperature must not be exceeded during board assembly at the customer's facility.

If moisture-sensitive components have been exposed to ambient air for longer than the specified time according to their MSL rating, or the humidity indicator card indicates too much moisture after opening a Moisture Barrier Bag (MBB), the components are required to be baked prior to the assembly process. Refer to imprints/labels on the respective packing to determine allowable maximum temperature.

The lower the MSL value, the less care is needed to store the components. The PQFN package MSL reliability is dependent upon the different supplier material set and package size. *Table 5* depicts the best case MSL for each package size at the time of this document's release. NXP packages use JEDEC standard IPC/JEDEC J-STD-020 for classification of its package.

---

**Table 4. MSL descriptions**

<table>
<thead>
<tr>
<th>Level rating</th>
<th>Floor life</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Time</td>
</tr>
<tr>
<td>1</td>
<td>Unlimited</td>
</tr>
<tr>
<td>2</td>
<td>1 year</td>
</tr>
<tr>
<td>2a</td>
<td>4 weeks</td>
</tr>
<tr>
<td>3</td>
<td>168 hours</td>
</tr>
<tr>
<td>4</td>
<td>72 hours</td>
</tr>
<tr>
<td>5</td>
<td>48 hours</td>
</tr>
<tr>
<td>5a</td>
<td>24 hours</td>
</tr>
<tr>
<td>7</td>
<td>TOL</td>
</tr>
</tbody>
</table>

TOL = Time on Label
Table 5. MSL capability of PQFN packages
(Note: This table and AN list all the NXP packages for which this AN applies, but some package types here maybe not available. Check with the NXP sales team)

<table>
<thead>
<tr>
<th>Package type</th>
<th>Body size</th>
<th>IO count</th>
<th>MSL</th>
<th>PPT (˚C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard PQFN</td>
<td>5x5</td>
<td>16</td>
<td>3</td>
<td>260</td>
</tr>
<tr>
<td></td>
<td>8x8</td>
<td>24</td>
<td>3</td>
<td>260</td>
</tr>
<tr>
<td></td>
<td></td>
<td>32</td>
<td>3</td>
<td>260</td>
</tr>
<tr>
<td></td>
<td>9x9</td>
<td>40</td>
<td>3</td>
<td>245</td>
</tr>
<tr>
<td>Custom PQFN</td>
<td>12x12</td>
<td>16</td>
<td>3</td>
<td>230 – 260</td>
</tr>
<tr>
<td></td>
<td></td>
<td>23</td>
<td>3</td>
<td>245 – 260</td>
</tr>
<tr>
<td></td>
<td></td>
<td>24</td>
<td>3</td>
<td>245 – 260</td>
</tr>
<tr>
<td></td>
<td></td>
<td>36</td>
<td>3</td>
<td>245</td>
</tr>
</tbody>
</table>
10 Package handling

10.1 Handling electrostatic discharge sensitive devices

Semiconductor Integrated Circuits (ICs) and components are Electrostatic Discharge Sensitive devices (ESDS), and proper precautions are required for handling and processing. Electrostatic Discharge (ESD) is one of significant factors leading to damage and failure of semiconductor ICs and components, and comprehensive ESD controls to protect ESDS during handling and processing should be considered. The following industry standards describe detailed requirements of proper ESD controls, and NXP recommends users meet the standards before handling and processing ESDS. Detail ESD specifications of devices are available in the device data sheet.

- JESD615-A - Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- IEC-101/61340-5 - Specification for the Protection of Electronic Devices from Electrostatic Phenomena

10.2 Handling moisture sensitive surface mount devices

PQFNs are Moisture/Reflow Sensitive Surface Mount Devices (SMD) and proper precautions are required for Handling, Packing, Shipping, and Use. Moisture from atmospheric humidity enters permeable packaging materials by diffusion. Assembly processes used to solder SMD packages to PCBs expose the entire package body to temperatures higher than 200 °C. As noted in Moisture sensitivity level, page 31, during solder reflow, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the package. Cracking and/or delamination can lead to failure and reliability concern, and proper handling of SMDs should be considered.

Dried Moisture Sensitive SMDs are placed in Tray or Tape and Reel, and dry packed for proper transportation and storage. SMDs are sealed with desiccant material and a Humidity Indicator Card inside of a MBB. Shelf life of dry packed SMDs are 12 months from the dry pack seal date when stored in < 40 °C/90 % RH environment.

Proper use and storage of Moisture Sensitive SMDs are required after MBB is opened. Improper use and storage increases various quality and reliability risks. SMDs that are subjected to reflow solder or other high temperature process must be mounted within the period of floor environment specified by MSL, or stored per J-STD-033B standard. Baking of SMDs is required before mounting if any of followings are experienced.

- SMDs exposed to specified floor environment greater than specified period
- Humidity Indicator Card reading > 10 % for level 2a - 5a or > 60 % for level 2 devices when read at 23 ± 5.0 °C environment.
- SMDs not stored according to J-STD-033B standard

Baking procedure, and more detailed requirements and procedures of handling Moisture Sensitive SMDs can be found in following industry standard.

- IPC/JEDEC J-STD-033B - Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

10.3 Packing of devices

PQFN devices are contained in Tray or Tape-and-Reel configurations, and Trays and Tape-and-Reels are dry packed for transportation and storage. Packing media are designed to protect devices from electrical, mechanical, and chemical damages as well as moisture absorption, but proper handling and storage of dry packs are recommended. Improper handling and storage (dropping dry packs, storage exceeding 40 °C/90 % RH environment, excessive stacking of dry packs, etc.) increases various quality and reliability risks.

- Tray
  - NXP complies with standard JEDEC tray design configuration - See Figure 41
  - Pin one of devices are oriented with lead one toward the chamfered corner of the tray
  - Trays designed to be baked for moisture sensitive SMDs, but temperature rating of tray should NOT be exceeded when devices are baked. Temperature rating can be found at end-tab of tray. Recommended baking temperature of trays is 125 °C.
  - Trays are typically banded together with 5+1 (five fully loaded trays and one cover tray) stacking and dry packed in Moisture Barrier Bag. Partial stacking (1+1, 2+1, etc.) is also available depending on individual requirements.
Figure 41. JEDEC tray example

- Tape and Reel
  - NXP complies with EIA-481D for carrier tape and reel configuration - See Figure 42 and Figure 43
  - NXP complies to Pin one orientation of devices with EIA-481D
  - Tape and Reels are NOT designed to be baked at high temperature
  - Each Tape and Reel is typically dry packed in Moisture Barrier Bag

Figure 42. Carrier tape specifications

- Dry Packing
• Trays and Tape-and-Reels, loaded with devices, are sealed in a moisture barrier bag which are labeled and packed in dedicated boxes with dunnage for the final shipment
• Each dry pack bag contains a desiccant pouch as well as a humidity indicator card
• NXP encourages the recycling and reuse of materials whenever possible.
• NXP will not use packing media items processed with or containing class 1 Ozone Depleting Substances
• Whenever possible, NXP shall design its packing configurations to optimize volumetric efficiency and package density to minimize the amount packing that enters the industrial waste stream
• NXP shall comply with following Environmental Standards Conformance guidelines / directives:
  – ISPM 15: Guidelines for regulating wood packaging material in international trade
11 References

[14] EIA-481, "Standards ? Excerpts used to assure complete alignment"
# 12 Revision history

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.0</td>
<td>12/2015</td>
<td>• Instituted revision history&lt;br&gt;• Complete rewrite</td>
</tr>
<tr>
<td></td>
<td>7/2016</td>
<td>• Updated to NXP document form and style&lt;br&gt;• Corrected minor typo errors</td>
</tr>
</tbody>
</table>