MSC8122 and MSC8126 Power Circuit Design Recommendations and Examples

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This application note discusses recommendations for designing power circuits to support correct power-up and power-down sequencing for MSC8122 and MSC8126 devices. The document discusses possible solutions using known board examples.

CONTENTS
1 MSC8122 and MSC8126 Power-Up Sequence ..2
2 On-Board 3.3 V and 1.2 V Power Regulators ....3
3 Migration of MSC8102 Designs.........................3
4 External 3.3 V Supply.........................................5
1 MSC8122 and MSC8126 Power-Up Sequence

The power-up sequence must follow the guidelines shown in Figure 1.

![Power-Up Sequence for VDDH and VDD/VCCSYN](image)

**Figure 1.** Power-Up Sequence for $V_{DDH}$ and $V_{DD}/V_{CCSYN}$

The following rules apply:

1. During time interval A, $V_{DDH}$ should always be equal to or less than the $V_{DD}/V_{CCSYN}$ voltage level. The duration of interval A should be kept below 10 ms.

2. The duration of timing interval B should be kept as small as possible and less than 10 ms.

**Note:** In the following sections, every reference to $V_{DD}$ also applies to $V_{CCSYN}$.

**Note:** Make sure that $V_{DD}$ is never greater than 0.8 V higher than $V_{DDH}$ during the power-up sequence. If the $V_{DD} - V_{DDH} > 0.8$ V, current can flow from the VDD supply to the VDDH supply through the ESD protection circuit. Use one of the following two methods to avoid the generation of this current:

- Design the circuits so that $V_{DD}$ can never rise to a level greater than $V_{DDH} + 0.8$ V.
- Add a current limiting resistor (10 $\Omega$ minimum) to GND for the $V_{DDH}$ supply. With such a design, when the $V_{DDH}$ supply is off, it has with an initial level of $V_{DD} - 0.8$ V.

See the product data sheet for power supply limits and specifications.
2 On-Board 3.3 V and 1.2 V Power Regulators

The following examples offers two possible on-board power supply designs that can support the recommended power-up sequence.

2.1 Two Regulators And a Power Monitor Unit

The preferred method of supplying sequenced power from on-board supplies is to use two power regulators operating in parallel and controlled by a power monitor unit as shown in Figure 1. The power monitor unit controls the order and timing of the power-up sequence. The advantage of using the power monitor is that you can tune the rise and fall of both supplies without reference to the individual loads on each supply.

![Figure 1. Two Parallel Regulators with Power Monitor](image)

**Note:** The power control unit should prevent \( V_{DD} \) from ever being > 0.8 V higher than \( V_{DDH} \).

2.2 Two Regulators with No Power Monitor

You can also use two regulators in parallel without a power monitor unit, as shown in Figure 3. You should verify that the design conforms to the recommended power-up/power-down design guidelines independent of the loading of the both regulators. You can also use the suggested solution in Section 3.

![Figure 3. Two Parallel Regulators with No Power Monitor](image)

**Note:** Make sure that \( V_{DD} \) is never greater than 0.8 V higher than \( V_{DDH} \) during the power-up sequence.

3 Migration of MSC8102 Designs

This example uses two regulators in parallel with a bias circuit as shown in Figure 4 similar to the one recommended for MSC8102 designs. In some configurations however, loading conditions can cause the regulator for \( V_{DDH} \) to raise the 3.3 V level first, which violates the MSC8122 power-up guidelines. To prevent this, use the
special circuit shown in Figure 5 between the source power supply, the 3.3 V regulator output, and the 1.2 V regulator output. The design was verified using one MSC8122 device and was shown to maintain the proper power-up sequence for the MSC8122 device.

As the supply voltage rises, base current drawn through resistor R1 turns transistor T1 off. Current from the 3.3 V supply moves to the core VDD rail and charges the on-board decoupling capacitors. When the voltage on the core VDD rail rises to ~0.8 V, current begins to pass through R2 and D1 to the base of T2. This current switches transistor T2 on, which connects ground to the base of the T1. The resulting ground level on the base of T1 switches off T1. The potential on the core VDD rail falls, and that closes T2 and opens T1. This state continues until the core VDD voltage regulator does not turn on and the voltages become stable.

Note: Make sure that VDD is never greater than 0.8 V higher than VDDH during the power-up sequence.
4 External 3.3 V Supply

\( V_{DDH} \) can be generated directly from an external 3.3 V supply, and the circuit can use a single voltage regulator to generate the \( V_{DD} \) for the core voltage as shown in Figure 6. Because the 3.3 V connects directly to the MSC8122 or MSC8126 device and \( V_{DD} \) is generated from the same source, application of the 3.3 V level should be delayed until the \( V_{DD} \) supply rises to its nominal level. The 3.3 V supply is controlled by a switch mechanism that does not close until \( V_{DD} \) is at the required voltage level. Refer to the technical data sheet for your device for the \( V_{DD} \) specifications.

![Figure 6. I/O Supply Using a Switching Element](image)

Figure 7 shows a block diagram of this configuration. The reference voltage needs to be checked against the \( V_{DD} \) core voltage. The switch should only open when \( V_{DD} \) rises to ~1.0 V.

![Figure 7. I/O Switching Example Block Diagram](image)

Figure 8 shows the circuit that was verified on a Freescale evaluation board.

![Figure 8. Tested Implementation of \( V_{DDH} \) Switch Logic](image)

In this example, the reference voltage is derived from the 1.2 V regulator output. The control of the high-side switch goes low when the 1.2 V regulator output voltage rises to 1.0 V. The MIC2505-2BM switch control (\( CTL \)) signal is active low.
Because the circuit shown in Figure 8 delays applying the 3.3 V to the MSC8122 device, there could be a potential problem with logical 1 inputs to the MSC8122 device from other parts on the board. To minimize this problem, we recommend that you use the switched 3.3 V for other system devices as well as the MSC8122 device so that the design supplies the 3.3 V power to all parts simultaneously.

If the design must use the switched 3.3 V power only with the MSC8122 device, you must consider the following:

- Each input that is driven to a 1 state during power-up may draw up to 80 mA. Compute the total possible power draw per input using the following equation:
  \[
  \text{current for one input pin} = \frac{(V_{DDH} - 0.7 \text{ V})}{(R_{driver} + R_{board} + 7 \Omega)}
  \]
  \[
  \text{Equation 1}
  \]
  where,
  - \(R_{driver}\) = the resistance of the driver circuit
  - \(R_{board}\) = the resistance of the board

  From the equation, it can be seen that any resistor put on board decreases the current draw.

- To minimize current through the inputs, drive all inputs to a logical 0 until the MSC8122 device \(V_{DDH}\) reaches its nominal level.

- Any pin that connects to MSC8122 devices on the board and drives a logical 1 causes current that increases according to the number of MSC8122 devices connected. The current draw for multiple MSC8122 devices being driven is:
  \[
  \text{current for shared input pins} = \frac{(V_{DDH} - 0.7 \text{ V})}{(R_{driver} + R_{board} + 7 \Omega/N)}
  \]
  \[
  \text{Equation 2}
  \]
  where,
  - \(R_{driver}\) = the resistance of the driver circuit
  - \(R_{board}\) = the resistance of the board
  - \(N\) = the total number of MSC8122 devices driven

- Connect unused input pins to their non-active value (pulled up or pulled down) via resistors.
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