Overview

The 56F807 is a member of the 56800 core-based family of digital signal controllers. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller (MCU) with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility and compact program code, the 56F807 is well-suited for many applications. The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for compilers to enable rapid development of optimized control applications.

Energy Information

> Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
> Uses a single 3.3V power supply
> On-chip regulators for digital and analog circuitry to lower cost and reduce noise
> Wait and stop modes available
**56F807 16-bit Digital Signal Controller**

> Up to 40 MIPS at 80 MHz core frequency
> DSP and MCU functionality in a unified, C-efficient architecture
> Hardware DO and REP loops
> MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
> 140 KB On-chip Flash
  > 120 KB Program Flash
  > 16 KB Data Flash
  > 4 KB Boot Flash
> 4 KB Program RAM
> 8 KB Data RAM
> Two 6-channel PWM modules
> Four 4-channel, 12-bit ADCs
> Two quadrature decoders
> CAN 2.0 A/B module
> Two SCIs
> SPI
> Four general-purpose quad timers
> JTAG/OnCE port for debugging
> 14 dedicated and 18 shared general-purpose input/output (GPIO) lines
> 160-pin LQFP or 160 MAPBGA packages

**56F807 Memory Features**

> Harvard architecture permits as many as three simultaneous accesses to program and data memory
> On-chip memory including a low-cost, high-volume Flash solution
  > 140 KB On-chip Flash
  > 120 KB Program Flash
  > 16 KB Data Flash
  > 4 KB Boot Flash
  > 4 KB Program RAM
  > 8 KB Data RAM
> Off-chip memory expansion capabilities
  > As much as 128 KB data memory
  > As much as 128 KB program memory

**56F807 Peripheral Circuit Features**

> Two PWM modules, each with six PWM outputs, three current sense inputs and four fault inputs; fault-tolerant design with dead-time insertion; supports both center- and edge-aligned modes
> Four 12-bit ADCs, which support two simultaneous conversions; ADC and PWM modules can be synchronized
> Two quadrature decoders
> Four dedicated general-purpose quad timers
> Two SCIs
> CAN 2.0 A/B module
> SPI
> Computer operating properly (COP)/watchdog timer
> Two dedicated external interrupt pins
> 14 dedicated GPIO pins, 18 multiplexed GPIO pins
> External reset input pin for hardware reset
> External reset output pin for system reset
> JTAG/OnCE for unobtrusive, processor speed-independent debugging
> Software-programmable, Phase-Lock Loop (PLL)-based frequency synthesizer

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**Award-Winning Development Environment**

> Processor Expert™ (PE) technology provides a rapid application design (RAD) tool that combines easy-to-use, component-based software application creation with an expert knowledge system.

> The CodeWarrior™ Integrated Development Environment (IDE) is a sophisticated tool for code navigation, compiling and debugging. A comprehensive set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE technology, the CodeWarrior tool suite and EVMs create a comprehensive, scalable tools solution for easy, fast and efficient development.

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