Digital Signal Processor

MSBA8100 Baseband Accelerator

The MSBA8100 is the market’s first multistandard baseband accelerator that supports the new wireless standards like 3G-LTE, WiMAX, HSPA+ and TDD-LTE. The device enables manufacturers of wireless infrastructure equipment to create substantially lower-cost, differentiated channel cards. Offering tremendous processing power while maintaining a competitive price and power, the MSBA8100 device accelerates tasks such as Turbo decoding, Viterbi decoding, fast fourier transform (FFT), inverse fast fourier transform (IFFT), discrete fourier transform (DFT) and inverse discrete fourier transform (IDFT). Targeted applications include next-generation standalone or unified 3G-LTE, WiMAX, HSPA+ and TDD-LTE and base stations.

The new MSBA8100 baseband accelerator meets the high performance, increased bandwidth and low latencies required to handle these high data rate standards. The Multi Accelerator Platform Engine for Baseband (MAPLE-B) consists of a programmable-system-interface (PSIF) that is a programmable controller with DMA capabilities and three accelerators attached using an internal interface: the Turbo/Viterbi Processing-Element (TVPE), the FFT Processing-Element (FFTPE) and DFT Processing-Element (DFTPE). The PSIF has two 64-bit wide MBus master ports used to transfer input and output data to and from system memory and a 64-bit MBus Slave port that allows any host to access its internal memories.

The MSBA8100 device also includes a large internal memory and supports a variety of advanced interface types, including two RapidIO® interfaces for data and control planes interfacing DSPs such as the MSC8144, switches and other ASICs or FPGAs, a PCI controller for easy configuration of the device and other control plane transactions, and a DDR controllers for high-speed, industry-standard memory interface. In addition to Turbo and Viterbi decoding, the MSBA8100 accelerates rate de-matching for various wireless standards and security algorithms. These include EDCH for 3GPP, sub-block de-interleaving and de-interlacing with HARQ support for 3G-LTE and WiMAX.

Eliminating the need to develop costly FPGA or custom ASIC devices, the baseband accelerator together with Freescale’s MSC8144 quad core DSP drives a range of base station designs. Fitted with advanced high-speed interfaces, the combined MSC8144 + MSBA8100 solution can be used for varied system topologies. Communication with the MSC8144 DSP and the antenna interface are accomplished through the two serial RapidIO® interfaces, each scalable up to 4 lanes at 3.125 Gbaud. In addition, the accelerator includes 512 Kb of internal memory. It also contains two flexible programmable RISC engines; the engines are pre-configured and can be reprogrammed in the future to accommodate updates.

Target Wireless Applications

- 3G-LTE
- TDD-LTE
- WiMAX
- HSPA
- 3GPP-R6
- 3GPP2
- TD-SCDMA
Features

- Multi Accelerator Platform Engine for Baseband (MAPLE-B)
  - Programmable System Interface with buffer descriptor based handshake/ task assignment, task prioritizations via multiple descriptor rings, processing element management and scheduling, two master buses for data transfers (up to 50 Gbps), slave bus for internal access, and job completion notification (interrupt or RapidIO doorbell and status bits)
  - Turbo decoding with scalable architecture with 1, 2 or 4 Radix-4 dual-recursion engines that supports WiMAX OFDMA turbo decoding, turbo decoding and 3GPP-R6 turbo decoding
  - Viterbi decoding that supports WiMAX OFDMA channel decoding, 3G-LTE (Evolved UTRA) channel decoding, and 3GPP-R6 Viterbi decoding
  - FFT/IFFT and DFT/IDFT Processing

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Key Advantages

- Convergence
  - Used with the MSC8144 to support both next-generation and legacy standards
  - Supports wireless baseband applications in standalone or unified base stations
  - Provides multi-standard baseband acceleration support for 3G-LTE, WiMAX, and HSPA+
  - Provides high performance, increased bandwidth and low latency to support high data rate operation
  - Chip-level arbitration and switching system (CLASS) that arbitrates between the MAPLE-B initiator buses, Serial RapidIO controllers, PCI controller initiator bus to the M2 memory, DDR SDRAM controller, MAPLE-B target bus, PCI target bus and the device configuration control and status registers (CCSRs)
  - 512 Kb M2 low-latency memory for critical data and temporary data buffering. Accessible at up to 400 MHz from all CLASS masters via four interleaved 64-bit ports
  - DDR Controller with up to 166 MHz clock rate (333 MHz data rate) and 16/32-bit DDR SDRAM data bus. Supports 64 MB to 4 GB DDR2 devices with x8/x16 data ports (no direct x4 support).

- Two serial RapidIO ports supporting 1x/4x operation up to 3.125 Gbaud, each containing a RapidIO messaging unit and a RapidIO DMA unit

- Cost Effectiveness
  - Eliminates the need for custom FPGAs or ASICs
  - Decreased time to market
  - With the MSC8144 provides a scalable system to support emerging standards and easily incorporate unique algorithms and intellectual property

- Compatibility
  - Designed for use with the MSC8144 DSP
  - Supports standard DDR2 memory
  - Provides standard Serial RapidIO interface for device interconnect

- PCI designed to be compliant with the PCI specification revision 2.2. Supports 33 MHz and 66 MHz 32-bit 3.3 V PCI interface, and PCI-to-system and system-to-PCI streaming.

- Three input clocks and four PLLs
- Four general-purpose input/output (GPIO) ports
- JTAG: Test Access Port (TAP) and Boundary Scan Architecture designed to comply with IEEE Std. 1149.1™
- Reduced power dissipation with low-power standby modes and optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)

- Technology: The MSBA8100 device is manufactured using CMOS 90 nm SOI technology

MSBA8100ADS Development System Simplifies Implementation

For rapid system prototyping and development, an MSBA8100ADS development board is available from Freescale, facilitating the development of software and the system in parallel. The board ships with the MSBA8100 device (connected to two 16-bit DDR memories) and the MSC8144 DSP both connected via the on-board 4x serial RapidIO switch.

Learn More: For more information about Freescale’s StarCore® DSPs, please visit www.freescale.com/starcore.