Implementing a 10-Bit Sigma-Delta Analog-to-Digital Converter Using the HC9S08Rx MCU Family Analog Comparator

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Introduction

Analog-to-digital (AD) converters, based on the Sigma-Delta (ΣΔ) modulation trade resolution in time for resolution in amplitude by combining:

- High sampling rates
- Negative feedback
- Digital filtering

First order ΣΔ AD comparators are the simplest, most robust, and have a stable modulator architecture. They are especially insensitive to circuit imperfections and component mismatch since they rely on a simple integrator and a comparator embedded within a feedback loop; whereas, the digital filter can be easily implemented with a comb filter.

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This application note describes how to implement a 10-bit first-order continuous-time $\Sigma \Delta$ AD converter using a member of the HC9S08Rx MCU Family of devices including the analog comparator feature. In spite of this MCU family not having a built-in AD converter the analog comparator, internal bandgap reference voltage and timers can be used to convert an analog input signal to the digital domain with 10-bits of resolution. Some members of the HC9S08Rx MCU Family have a rail-to-rail comparator module and their internal bandgap reference can be selected as the comparator reference voltage. The HC9S08Rx analog comparator allows developing a very low-cost first-order continuous-time $\Sigma \Delta$ modulator by adding a few external components; whereas, the MCU itself emulates the digital decimeter filter in software using its internal timers. High resolution can be attained by properly adjusting the input bandwidth and the oversampling ratio.

**$\Sigma \Delta$ Modulation at a Glance**

Figure 1 illustrates the basic architecture of a $\Sigma \Delta$ AD converter comprising:

- An analog integrator
- A quantizer or comparator enclosed in a feedback loop via a single-bit digital-to-analog (DA) converter
- A digital low-pass filter.

The input signal is fed to the comparator through the integrator and the quantized output is fed back and subtracted from the input. This feedback forces the average value of the quantized signal to track the average input. Any difference between them accumulates in the integrator and eventually corrects itself. Jointly with the integrator, the feedback loop attenuates the quantization noise at low frequencies while shaping the noise power to the high frequency range. Since the signal is sampled at a frequency greater than the Nyquist rate, high frequency noise can be removed without affecting the signal band by means of a digital low-pass filter operating at the output of the $\Sigma \Delta$ modulator.
Figure 2 exhibits the response of the modulator to a ramp input signal. Note the quantized output oscillates in such a manner that its local average equals the average input. The digital data coming from the modulator is a single bit stream of 1’s and 0’s and the density of digital 1’s is proportional to the average value of the input signal. The high frequency data from the modulator is then low-pass filtered in order to remove any shaped noise and to decimate to the Nyquist rate. This decimation results in an n-bits binary output format.

ΣΔ modulators have been widely implemented in the discrete-time domain using switched-capacitor circuits. However, continuous-time ΣΔ modulators have become very popular since their performance is similar to the discrete-time version. Figure 3 shows a first order continuous-time ΣΔ AD converter where the R1-C1 network acts as a passive integrator; whereas, the resistor R2 works as a 1-bit DA converter closing the feedback loop. The R1-C1 circuit also performs low-pass anti-alias filtering on the AD converter input.

![ΣΔ Modulator Output Bit Stream](image)

**Figure 2. Response of the ΣΔ Modulator to a Ramp Input Signal**

Defining the oversampling ratio as:

\[ M = \frac{f_{CK}}{f_N} \]  

where:

- \( f_{CK} \) is the clock sampling frequency
- \( f_N \) is the Nyquist rate for a signal bandwidth of \( f_{In} \) (\( f_N = 2 f_{In} \))

The signal-to-noise ratio (SNR) of the first order ΣΔ modulator is given by:

\[ \text{SNR} = 30 \log M - 3.41 \text{ dB} \]  

Equation 2

From equation 2, providing the oversampling ratio is larger than approximately 130, the circuit in Figure 3 allows attaining a 10-bit resolution. Since for DC or slowly varying input signals the noise power has large peaks degrading the ΣΔ modulator SNR, a high frequency dither signal uncorrelated with the input should be injected. It has the effect of redistributing the energy present in the noise peaks over the entire amplitude range maintaining the expected resolution given by equation 2.
Implementation with HC9S08Rx MCU Family

The HC9S08Rx MCU with the analog comparator function can be configured as a first-order continuous-time $\Sigma\Delta$ AD converter as depicted in Figure 4. This is done by adding:

- Two external resistors
- One capacitor
- Properly programming the internal timers to filter and decimate the comparator digitized output.

![First-Order Continuous-Time $\Sigma\Delta$ AD Converter Implementation](image)

The $R_1$-$C_1$ integrator is similar to the $\Sigma\Delta$ modulator in Figure 3. The 1-bit DA conversion is achieved by driving the resistor $R_2$ with an output buffer. The resistors must be adjusted to allow full range operation avoiding the integrator saturation. A suitable capacitor value must be adjusted regarding the sampling frequency and the input signal bandwidth. Once again, the $R_1$-$C_1$ network provides low-pass filtering with the option to include an additional anti-alias analog filter.

One internal HC9S08Rx MCU timer accumulates the number of 1’s (or 0’s) at the output of the comparator to compute the average of the analog input signal. A second timer controls the number of accumulator counts. Each accumulator increment is carefully controlled by software and it defines the $\Sigma\Delta$ modulator sampling frequency and then the oversampling ratio $M$. To achieve a 10-bit output word length, the accumulator must sample 1024 times the input signal. Therefore, the conversion time increases when a more accurate solution is required.
First Order Continuous-Time $\Sigma\Delta$ AD Converter Characteristics

$\Sigma\Delta$ AD converter characteristics include:

- Low cost implementation with few external components
- Low complexity especially in the analog domain since the HC9S08Rx MCU itself provides the digital processing capacity needed
- Small amount of memory required
- Input range controlled by external resistors
- Low matching level in between external components
- Performance immunity face-to-comparator hysteresis
- Modulator highly robust and inherently stable
- Accurate internal bandgap reference voltage
- Converter inherently linear and inherently monotonic
- Very simple anti-alias low-pass filter feasible to embed with the RC passive integrator
- Sample and hold, and trimming circuitry not required
- Architecture not particularly appropriate for DC inputs but for busy signals
- DC input applications require radiometric measurements and dithering
- 61.2 dB of SNR equivalent to 10-bits resolution
- 65.7 dB of dynamic range (DR) at 2.4 V of power supply

HC9S08Rx Features and Benefits

Standard features of the HCS08 Family

- Extended battery life technology
  - Multiple power management modes including 20 nA power down @ 2 V
  - Optional auto wake-up with internal timer and internal oscillator typically 700 nA @ 2 V
  - 1.8–3.6 V operation
- High-performance when needed
  - 125 ns minimum instruction cycle time down to 1.8 V @ 8 MHz bus
- Innovative on-chip trigger/trace debug capability
  - Single wire background debug mode
  - Trace capability with 9 trigger modes and 3 breakpoints

Features of the MC9S08RC/RD/RE/RG MCU Family

- 8 MHz internal bus frequency
- On-chip in-circuit programmable FLASH memory with block protection and security option
- On-chip random-access memory (RAM)
- Low power oscillator capable of operating from crystal or resonator from 1 to 16 MHz
Devices in the MC9S08RC/RD/RE/RG Series

Table 1. MC9S08RC/RD/RE/RG Series Devices

<table>
<thead>
<tr>
<th>Device</th>
<th>FLASH</th>
<th>RAM(1)</th>
<th>ACMP(2)</th>
<th>SCI</th>
<th>SPI</th>
</tr>
</thead>
<tbody>
<tr>
<td>9S08RG32/60</td>
<td>32K/60K</td>
<td>2K/2K</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>9S08RE8/16/32/60</td>
<td>8K/16K/32K/60K</td>
<td>1K/1K/2K/2K</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>9S08RD8/16/32/60</td>
<td>8K/16K/32K/60K</td>
<td>1K/1K/2K/2K</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>9S08RC8/16/32/60</td>
<td>8K/16K/32K/60K</td>
<td>1K/1K/2K/2K</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>

NOTES:
1. Three S08RC/RD/RE16 ROM MCU devices have 512 bytes RAM instead of 1K bytes.
2. Only available in 32- or 44-pin LQFP packages.
Application Description

Figure 5 shows the schematic diagram of the 10-bit ΣΔ AD converter using a MC9S08Rx MCU including the analog comparator feature. Assuming the system employs two NiCd batteries of 1.2 V and the full input signal range is to be 2.4 V, R1 and R2 must be set to 47 kΩ to prevent integrator saturation. Since these resistors are not critical, carbon composition resistors or metal film resistors with 5% tolerance can be used. C1 is a ceramic capacitor. Its value depends on the modulator sampling frequency and oversampling ratio. The modulator sampling frequency is the MCU bus clock frequency divided by the number of cycles required to run the software instructions. As mentioned in Software Description, the modulator sampling frequency can be set to 50 kHz adjusting properly the timer interruption as a function of the 8-MHz bus clock. Therefore, for an oversampling ratio of 130, the input signal bandwidth is limited to be 190 Hz and the integrator capacitor should be below 18 nF.

Figure 5. First-Order Continuous-Time ΣΔ AD Converter Circuit Diagram

Typically, application systems have two separate capacitors across the power pins. In this case there should be a bulk electrolytic capacitor, such as a 1-µF tantalum capacitor, to provide bulk charge storage for the overall system and a 0.1-µF ceramic bypass capacitor located as close to the MCU power pins as practical to suppress high-frequency noise.

The MCU oscillator is a traditional Pierce oscillator that can accommodate a crystal or ceramic resonator up to 16 MHz. Resistor R3 should be a low-inductance resistor such as a carbon composition resistor and it’s tolerance is not critical. C2 and C3 should be ceramic capacitors being typically in the 5-pF to 25-pF range and are chosen to match the requirements of a specific crystal or resonator. The crystal

Implementing a 10-Bit Sigma-Delta Analog-to-Digital Converter Using the HC9S08Rx MCU Family Analog Comparator, Rev. 0.1
Application Description

manufacturer typically specifies a load capacitance that is the series combination of C2 and C3 that are usually the same size.

Figure 6 illustrates the typical ΣΔ modulator output when a ramp signal is applied to the input. Note the density of digital 1’s is proportional to the average input. If the input is just about the internal bandgap reference voltage the output signal oscillates at half the modulator sampling frequency. That is known as the idle pattern. Figure 7 and Figure 8 exhibit the typical ΣΔ modulator response to triangle and sinusoidal input signals, respectively.

Figure 6. First-Order Continuous-Time ΣΔ Modulator Response to a Ramp Input Signal

Figure 7. ΣΔ Modulator Response to a Triangle Input Signal
The $\Sigma\Delta$ modulator evaluation is performed by analyzing the single-bit output signal spectrum through the Fast Fourier Transform (FFT). Input power is normalized to the quantization step defined by the comparator supply voltage whereas the sampling rate is set to 128 kHz with the timer interruption feature. Figure 9 shows the output spectrum for a 125 Hz sinusoidal input signal with –8 dB of normalized power.

**NOTE**

The noise shaping concentrates the noise power in the high frequency range of the spectrum.

The spectrum detail in Figure 10 demonstrates a SNR of 55 dB for a –8 dB input power.

Figure 11 shows the measured $\Sigma\Delta$ modulator SNR versus the input signal amplitude. Extrapolating from the data of Figure 11, the measured dynamic range of the AD converter is found to be 65.7 dB and its maximum SNR is 61.2 dB. For large input signals, the precision of the converter is limited by quantization noise and harmonic distortion as apparent from the output spectrum in Figure 9 and Figure 10. The 10-bit digital output is monotonically linear as expected.
Figure 9. Measured Output Spectrum of the First-Order Continuous-Time $\Sigma\Delta$ Modulator
Figure 10. Measured Baseband Output Spectrum with -8 dB Sinusoidal Input Power

Figure 11. Measured $\Sigma \Delta$ Modulator SNR for a 50-kHz Sampling Frequency and 125-Hz Input Signal Frequency
Two software options are listed in this application note. The first one is intended to implement a first-order continuous-time $\Sigma\Delta$ modulator according to the flowchart in Figure 12. The second one corresponds to the complete first-order continuous-time $\Sigma\Delta$ AD converter in Figure 5 and its flowchart is depicted in Figure 13.

**Figure 12. The First-Order $\Sigma\Delta$ Modulator Software Flowchart**
Figure 13. The Complete First-Order $\Sigma\Delta$ AD Converter Software Flowchart
Software Description

The continuous-time $\Sigma\Delta$ modulator software:

- Configures the I/O ports and registers
- Sets the timer interrupt to a 128-kHz frequency
- Clears PTE0 and the MCU stays in wait mode until an interrupt is reached.
- After the timer overflows, PTE0 is set high and the comparator output flag (ACO) is verified.
  - If ACO is set, PTA1 and PTA2 are also set high
  - When ACO is cleared, PTA1 and PTA2 are cleared as well
- Code returns to wait mode and the process stays in a loop

The $\Sigma\Delta$ AD converter software:

- Comprises both the modulator and the filter codes
- Configures the I/O ports and registers
- Sets the timer interrupt to occur periodically at a 60-kHz frequency
- Clears counter and result variables and the program enters wait mode
- Verifies the modulator routine ACO
- The difference between the codes is:
  - When ACO is set, PTA1 and PTA2 are also set and the result is incremented.
  - If ACO is cleared, PTA1 and PTA2 are cleared as well but the result is not incremented.
- The next step is to increment the counter and check its value.
  - If counter is less than 1024, decimal, the program returns to wait mode.
  - Otherwise, when the counter is at 1024, PTB and PTC ports output the AD conversion result.
- Both counter and results are cleared and the program returns to wait mode
Software Listings

SigmaDeltaM.asm

;*******************************************************************************
;* Title: SigmaDeltaM.asm (c) Freescale Inc. 2004 All rights reserved.
;*******************************************************************************
;* Author: Marcus Espindola - Freescale SPS/BSTC
;*******************************************************************************
;* Description: Implementing a 10-bit Sigma-Delta Analog to Digital Converter Using the
;*              HC9S08Rx MCU Family Analog Comparator - Code for Sigma-Delta Modulator
;*******************************************************************************
;* Documentation: 9S08RC16 Data Sheet for register and bit explanations
;*******************************************************************************
;* Include Files: 9S08RC16.equ, SigmaDelta.equ
;*******************************************************************************
;* Assembler: P&E Microcomputer Systems - CASM for HC08 and
;*            CodeWarrior 3.0
;*******************************************************************************
;* Revision History:
;* Rev #   Date      Who         Comments
;* -----   -----------  ---------   --------------------------------------------
;* 1.0     29-Jan-04  Espindola   Initial data entry
;*----------------------------------------------------------------------
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;*******************************************************************************

; XDEF Entry,Reset,TPMInt

;*******************************************************************************
;* Equates and Data Table Includes
;*******************************************************************************

include "9S08RC16.equ"

;DEFAULT_RAM          SECTION SHORT

org   RamStart

Implementing a 10-Bit Sigma-Delta Analog-to-Digital Converter Using the HC9S08Rx MCU Family Analog Comparator,
Rev. 0.1
;*******************************************************************************************
;* Constants and Variables for this file
;*******************************************************************************************
include 'SigmaDelta.equ'

;DBFAULT_ROM       SECTION

;*******************************************************************************************
;* Code Section
;*******************************************************************************************

org   FlashStart

Entry:
Reset:      ldhx  #RamEndAddress+1     ; H:X = #RamEndAddress + 1
           txs                        ; Stack Pointer (SP) = #RamEndAddress
           lda   #setSIMOPT
           sta   SIMOPT               ;configure SIMOPT register
           lda   #setPMCSC1
           sta   PMCSC1               ;configure PMCSC1 register
           mov   #setACMPSC,ACMPSC    ;configure analog comparator
           clr   TPMCNTH
           clr   TPMCNTL              ;reset TPM counter
           mov   #setTPMMODH,TPMMODH  
           mov   #setTPMMODL,TPMMODL  ;a Timer interrupt will be generated every TPMMOD
           bset  TOIE,TPMSC           ;Timer Overflow Interrupt Enable = 1
           bset  CLKSA,TPMSC          ;Clock Source Select = BUSCLK
           bcir  PTA1,PTA             ;clear bit 1 of port PTA
           bcir  PTA2,PTA             ;clear bit 2 of port PTA
           bset  DDRA1,DDRA           ;define bit 1 of port PTA as output
           bset  DDRA2,DDRA           ;define bit 2 of port PTA as output
           bcir  PTE0,PTE             ;clear bit 0 of port PTE
           bset  DDB0,DDRE            ;define bit 0 of port PTE as output

WaitState:  bcir  PTE0,PTE
            wait                     ;enable interrupts and halt
            bra   WaitState

;*******************************************************************************
;* Timer Interrupt
;*******************************************************************************

TPMInt:  lda  TPMSC     ;read TPMSC register (required before clearing TOF)
bclr TOF,TPMSC          ;clear Timer Overflow Flag

    bset  PTE0,PTE        ;set bit 0 of port PTE
    brset ACO,ACMPSC,SetOutHigh ;jump to SetOutHigh if ACO == 1

    bclr  PTA1,PTA        ;clear bit 1 of port PTA
    bclr  PTA2,PTA        ;clear bit 2 of port PTA
    rti                      ;return from interrupt routine

SetOutHigh: bset  PTA1,PTA     ;set bit 1 of port PTA
            bset  PTA2,PTA     ;set bit 2 of port PTA
            rti                      ;return from interrupt routine

END
Software Listings

SigmaDeltaF.asm

;*******************************************************************************************
;* Title: SigmaDeltaF.asm (c) Freescale Inc. 2004 All rights reserved.
;*******************************************************************************************
;* Author: Marcus Espindola - Freescale SPS/BSTC
;*******************************************************************************************
;* Description: Implementing a 10-bit Sigma-Delta Analog to Digital Converter Using the
;* HC9S08Rx MCU Family Analog Comparator - Code for Sigma-Delta A2D Coverter
;*******************************************************************************************
;* Documentation: 9S08RC16 Data Sheet for register and bit explanations
;*******************************************************************************************
;* Include Files: 9S08RC16.equ, SigmaDelta.equ
;*******************************************************************************************
;* Assembler: P&E Microcomputer Systems - CASM for HC08 and
;* CodeWarrior 3.0
;*******************************************************************************************

;*******************************************************************************************
;** Revision History:
;* Rev # Date Who Comments
;* -------  ------- --------- --------------------------------------------
;* 1.0  29-Jan-04 Espindola Initial data entry
;*******************************************************************************************

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;       XDEF Entry,Reset,TPMInt

;*******************************************************************************************
;** Equates and Data Table Includes
;*******************************************************************************************

include "9S08RC16.equ"

;DEFUALT_RAM       SECTION SHORT

org   RamStart

Implementing a 10-Bit Sigma-Delta Analog-to-Digital Converter Using the HC9S08Rx MCU Family Analog Comparator,
Rev. 0.1
;*****************************************************************************
;* Constants and Variables for this file
;*****************************************************************************

include 'SigmaDelta.equ'

;DBFAULT_ROM    SECTION

;*****************************************************************************
;* Code Section
;*****************************************************************************

org   FlashStart

Entry:
Reset: ldhx #RamEndAddress+1 ; H:X = #RamEndAddress + 1
txs ; Stack Pointer (SP) = #RamEndAddress
lda #setSIMOPT
sta SIMOPT ;configure SIMOPT register

lda #setPMCSC1
sta PMCSC1 ;configure PMCSC1 register

mov #setACMPSC,ACMPSC;configure analog comparator

clr TPMCNTH ;reset TPM counter
clr TPMCNTL

mov #setTPMMDH,TPMMDH
mov #stTPMMDL,TPMMDL ;a Timer interrupt will be generated every TPMMOD
                      ;BUSCLKs (133 -> ~60kHz)

bset TOIE,TPMSC ;Timer Overflow Interrupt Enable = 1
bset CLKSA,TPMSC ;Clock Source Select = BUSCLK

bcir PTA1,PTA ;clear bit 1 of port PTA
bcir PTA2,PTA ;clear bit 2 of port PTA
bset DDRA1,DDRA ;define bit 1 of port PTA as output
bset DDRA2,DDRA ;define bit 2 of port PTA as output

clr PTB ;reset port PTB
clr PTC ;reset port PTC

mov #OutPorts,DDRB ;define port PTB as output
mov #OutPorts,DDRC ;define port PTC as output

clr CounterL ;reset Counter (low order)
clr CounterH ;reset Counter (high order)
clr SampleL ;reset Sample (low order)
clr SampleH ;reset Sample (high order)

bcir PTE0,PTE ;clear bit 0 of port PTE
bcir PTE1,PTE ;clear bit 1 of port PTE
bset DDRD0,DDRE ;define bit 0 of port PTE as output
bset DDRD1,DDRE ;define bit 1 of port PTE as output

Implementing a 10-Bit Sigma-Delta Analog-to-Digital Converter Using the HC9S08Rx MCU Family Analog Comparator,
Rev. 0.1

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Software Listings

WaitState:  
wait              ;enable interrupts and halt (2+ cycles)
bclr  PTE0,PTE    ;clear bit 0 of port PTE (5 cycles)
bra  WaitState    ;jump to WaitState (3 cycles)  --> Total = 10+ cycles

;*******************************************************************************************
;* Timer Interrupt (min = 48 cycles / max = 108 cycles)
;*******************************************************************************************

TPMInt:     
lda   TPMSC       ;read TPMSC register (required before clearing TOF) (3 cycles)
bclr  TOF,TPMSC   ;clear Timer Overflow Flag (5 cycles)
bset  PTE0,PTE    ;set bit 0 of port PTE (5 cycles)
brset ACO,ACMPSC,SetOutHigh  ;jump to SetOutHigh if ACO == 1 (5 cycles)
bclr  PTA1,PTA    ;clear bit 1 of port PTA (5 cycles)
bclr  PTA2,PTA    ;clear bit 2 of port PTA (5 cycles)
bra   IncCounter   ;jump to IncCounter (3 cycles)

SetOutHigh:  
bset  PTA1,PTA    ;set bit 1 of port PTA (5 cycles)
bset  PTA2,PTA    ;set bit 2 of port PTA (5 cycles)
inc   SampleL     ;increment Sample (low order) (5 cycles)
bne   IncCounter   ;jump to IncCounter if SampleL did not overflow (3 cycles)
inc   SampleH     ;increment Sample (high order) (5 cycles)

IncCounter: inc   CounterL    ;increment Counter (low order) (5 cycles)
bne  TPMIntEnd    ;jump to TPMIntEnd if CounterL did not overflow (3 cycles)
inc   CounterH    ;increment Counter (high order) (5 cycles)
brclr 2,CounterH,TPMIntEnd  ;jump to TPMIntEnd if Counter < 1024 ( 5 cycles)

bcitr  PTE1,PTE   ;clear bit 1 of port PTE (5 cycles)
mov   SampleL,PTB ;PTB = CounterH (5 cycles)
mov   SampleL,PTC ;PTC = CounterL (5 cycles)
bset  PTE1,PTE    ;set bit 1 of port PTE (5 cycles)
clr   CounterL    ;reset Counter (low order) (5 cycles)
clr   CounterH    ;reset Counter (high order) (5 cycles)
clr   SampleL    ;reset Sample (low order) (5 cycles)
clr   SampleH    ;reset Sample (high order) (5 cycles)

TPMIntEnd:  rti               ;return from interrupt routine (9 cycles)

END

Implementing a 10-Bit Sigma-Delta Analog-to-Digital Converter Using the HC9S08Rx MCU Family Analog Comparator,
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**SigmaDelta.equ**

;*******************************************************************************************
;* Title: SigmaDelta.equ
;* Copyright (c) Freescale 2004
;*******************************************************************************************
;* Author: Marcus Espindola - Freescale SPS/BSTC
;*******************************************************************************************
;* Description: Constants and variables definitions for 9S08RC16.
;*******************************************************************************************
;* Documentation: 9S08RC16 Data Sheet for register and bit explanations
;*******************************************************************************************
;* Include Files:
;*******************************************************************************************
;* Assembler: P&E Microcomputer Systems - CASM for HC08 and CodeWarrior 3.0
;*******************************************************************************************
;* Revision History:
;*******************************************************************************************
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;*******************************************************************************************
;* Constants and Variables for this file
;*******************************************************************************************
;*******************************************************************************************
; org RamStart

SampleH:  rmb  1
SampleL:  rmb  1

CounterH:  rmb  1
CounterL:  rmb  1

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Software Listings

setSIMOPT: equ $01000001 ;System Options Register
;
;       +---RESET Pin Enable = 1
;       +---Background Debug Mode Pin Enable = 0
;       +---Unused during write
;       +---Unused during write
;       +---Unused
;       +---Stop Mode Enable = 0
;       +---COP Watchdog Timeout = Long Timeout
;       +---COP Watchdog Enable = 0

setPMCSCL: equ $01011000 ;System Power Management Status and Control 1 Register
;
;       +---Unused during write
;       +---Unused during write
;       +---Unused during write
;       +---Low-Voltage Detect Reset Enable = 1
;       +---SAFE System from interrupts = 1
;       +---Clear Low-Voltage Detect Flag
;       +---Unused during write

setACMPSC: equ $11100011 ;ACMP Status and Control Register
;
;       +---Comparator output either rising or falling edge
;       +---Comparator output either rising or falling edge
;       +---Unused during write
;       +---Unused during write
;       +---Analog Comparator Interrupt Enable = 0
;       +---Clear Analog Comparator Flag
;       +---Analog Comparator Bandgap Select = 1
;       +---Analog Comparator Module Enable = 1

setTPMMODH: equ $00 ;Timer Counter Modulo High Register value
setTPMMOLDL: equ $3E ;Timer Counter Modulo Low Register value for modulator
stTPMMODLF: equ $85 ;Timer Counter Modulo Low Register value for filter

OutPorts: equ $FF ;Set ports as output

;*********************************************************************************
* Interrupt Vector Table
;*********************************************************************************
org $FFF2 ;Timer Overflow Interrupt Vector
fdb TPMInt
org $FFFE ;Reset Interrupt Vector
fdb Reset

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