Hardware Design Guidelines for S12ZVC
MagniV Mixed-Signal MCUs for CAN Applications

By: Jesús Sánchez

1 Introduction

1.1 Purpose and scope
This document contains hardware guidelines for designing with the S12ZVC family of S12 MagniV Mixed-signal MCUs from NXP. This includes:

- Device Overview S12ZVC Microcontroller
- Pin I/O overview
- Power Management
- RESET
- BKGD
- TEST Pin
- ADC Module
- DAC Module
- Analog Comparator
- High Voltage Input
- High and Low side Driver
- SENT Transmitter Interface

NOTE
Electrical parameters mentioned in this application note are subject to change in individual device specifications. Check each application against the latest data sheet for specific target devices.
2 S12ZVC device family overview

The MC9S12ZVC-Family is a new member of the S12 MagniV product line integrating a battery level (12 V) voltage regulator, supply voltage monitoring, high voltage inputs, and a CAN physical interface. It’s primarily targeted at CAN nodes like sensors, switch panels, or small actuators. It offers various low power modes and wakeup management to address state-of-the-art power consumption requirements.

Some members of the MC9S12ZVC-Family are also offered for high temperature applications requiring AEC-Q100 Grade 0 (-40°C to +150°C ambient operating temperature range). The MC9S12ZVC-Family is based on the enhanced performance, linear address space S12Z core and delivers an optimized solution with the integration of several key system components into a single device, optimizing system architecture, and achieving significant space savings.

2.1 MC9S12ZVC-Family comparison

Table 1 provides a summary of the MC9S12ZVC-Family. This information is intended to provide an understanding of the range of functionality offered by this microcontroller family.

<table>
<thead>
<tr>
<th>Feature</th>
<th>S12ZVCA</th>
<th>S12ZVCA</th>
<th>S12ZVC</th>
<th>S12ZVC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>192</td>
<td>128</td>
<td>96</td>
<td>64</td>
</tr>
<tr>
<td>Package option</td>
<td>64-pin LQFP-EP</td>
<td>48-pin LQFP</td>
<td>64-pin LQFP-EP</td>
<td>48-pin LQFP</td>
</tr>
<tr>
<td>Core</td>
<td>S12Z</td>
<td>S12Z</td>
<td>S12Z</td>
<td>S12Z</td>
</tr>
<tr>
<td>Flash memory (ECC) [KByte]</td>
<td>192</td>
<td>128</td>
<td>96</td>
<td>64</td>
</tr>
<tr>
<td>EEPROM (ECC) [KByte]</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>(4-byte erasable)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RAM (ECC) [KByte]</td>
<td>12</td>
<td>8</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>High Speed CAN Physical Layer</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>High Voltage Inputs</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Vreg for CAN PHY with ext. ballast (BCTLC)</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>VDDX/VSSX pins</td>
<td>2/2</td>
<td>2/2</td>
<td>2/2</td>
<td>2/2</td>
</tr>
<tr>
<td>msCAN</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SCI</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Feature</td>
<td>S12ZVCA 192</td>
<td>S12ZVCA 128</td>
<td>S12ZVCA 96</td>
<td>S12ZVCA 64</td>
</tr>
<tr>
<td>-------------------------------</td>
<td>------------</td>
<td>------------</td>
<td>------------</td>
<td>------------</td>
</tr>
<tr>
<td>SPI</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>IIC</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SENT (Transmitter)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>16-bit Timer channels</td>
<td>8</td>
<td>4</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>16-bit Timer channels (20 ns resolution)</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>16-bit PWM channels (20 ns resolution)</td>
<td>4</td>
<td>3</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>16-bit PWM channels</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>12-bit ADC channels</td>
<td>16</td>
<td>10</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>10-bit ADC channels</td>
<td>-</td>
<td>-</td>
<td>16</td>
<td>10</td>
</tr>
<tr>
<td>8-bit DAC</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>ACMP 5V (with rail-to-rail inputs)</td>
<td>2</td>
<td>2</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>EVDD (20 mA source)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Open Drain (5V GPIOs with disabled (PMOS))</td>
<td>10</td>
<td>5</td>
<td>10</td>
<td>5</td>
</tr>
<tr>
<td>N-GPIO (25mA sink)</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>General purpose I/O</td>
<td>42</td>
<td>28</td>
<td>42</td>
<td>28</td>
</tr>
</tbody>
</table>

1. at 25 MHz bus frequency
2.2 MC9S12ZVC-Family block diagram

Block Diagram shows the maximum configuration
Not all pins or all peripherals are available on all devices and packages.
Rerouting options are not shown.

Figure 1. High-level block diagram of the MC9S12ZVC-Family
3 Power management

The power and ground pins are described in subsequent sections.

3.1 VSUP – Main power supply pin

VSUP is the 12 V/18 V supply voltage pin for the on chip voltage regulator. This is the voltage supply input from which the voltage regulator generates the on chip voltage supplies. It must be protected externally against a reverse battery connection, as shown in Figure 2.

The designer could choose to add Bulk/Bypass capacitor as a charge tank to provide power when losing battery. The value of this capacitor depends on the current consumption and the amount of time the MCU needs to perform house-keeping activities before shutting down.

3.2 Digital I/O and analog supplies

3.2.1 VDDX, VSSX — Pad supply pins

VDDX is the supply domain for the digital Pads. An off-chip stability and decoupling capacitor between VDDX and VSSX are required. This supply domain is monitored by the Low Voltage Reset circuit. VDDX has to be connected externally to VDDA.

NOTE
All VDDX pins of the microcontroller (VDDX1 and VDDX2) must be connected together.

3.2.2 VDDA, VSSA — Regulator reference supply pins

VDDA and VSSA pins are used to supply the analog parts of the regulator. Internal precision reference circuits are supplied from these signals. An off-chip decoupling capacitor between VDDA and VSSA is required and can improve the quality of this supply. VDDA has to be connected externally to VDDX.

3.2.3 BCTL — Base control pin for external PNP

The device supports the use of an external PNP to supplement the VDDX supply, for reducing on chip power dissipation. In this configuration, most of the current flowing from VBAT to VDDX, through the external PNP. The BCTL pin is the ballast connection for the on chip voltage regulator for the VDDX/VDDA power domains. It provides the base current of an external PNP Ballast transistor. An additional resistor between emitter and base of the BJT is required.
NOTE
All GROUND pins of the microcontroller (VSSX1, VSSX2, VSSC, VSSA and VSS) must be connected together.

Table 2. VDDX/VDDA - Component description and recommended values

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>D_{RBP}</td>
<td>Reverse Current/Battery diode Protection</td>
<td></td>
</tr>
<tr>
<td>C_{BULK}</td>
<td>Bulk/Bypass capacitor</td>
<td></td>
</tr>
<tr>
<td>C_{DCP}</td>
<td>Decoupling Capacitor</td>
<td></td>
</tr>
<tr>
<td>Q_{PNPX}</td>
<td>PNP Ballast transistor</td>
<td></td>
</tr>
<tr>
<td>R_{BCTL}</td>
<td>Metal Film resistor</td>
<td>1 kΩ</td>
</tr>
<tr>
<td>C_{BT}</td>
<td>Stability Capacitor. X7R Ceramic or Tantalum</td>
<td>4.7 μF – 10 μF</td>
</tr>
<tr>
<td>C_{DDX1}, C_{DDX2}</td>
<td>Decoupling Capacitor for VDDX. X7R Ceramic</td>
<td>100 nF - 220 nF</td>
</tr>
<tr>
<td>C_{DDA}</td>
<td>Decoupling Capacitor for VDDA. X7R Ceramic</td>
<td>100 nF - 220 nF</td>
</tr>
</tbody>
</table>

3.3 CAN power supply

A supply for an external CANPHY is offered via external device pins BCTLC and VDDC, whereby BCTLC provides the base current of an external PNP and VDDC is the CANPHY supply (output voltage of the external PNP).

3.3.1 VDDC— CAN supply pin

VDDC is the supply domain for the CAN module. An off-chip Stability and decoupling capacitor between VDDC and VSSX is required. This supply domain is monitored by the Low Voltage Reset circuit.
3.3.2 BCTLC — Base control pin for external PNP for VDDC power domain

BCTLC is the ballast connection for the on chip voltage regulator for the VDDC power domain. It provides the base current of an external BJT (PNP) of the VDDC supply. An additional resistor between emitter and base of the BJT is required.

![BCTLC Diagram](image)

**Figure 3. VDDC - CAN Supply pin**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q&lt;sub&gt;PNPC&lt;/sub&gt;</td>
<td>PNP Ballast transistor</td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;BCTLC&lt;/sub&gt;</td>
<td>Metal Film resistor</td>
<td>1 kΩ</td>
</tr>
<tr>
<td>C&lt;sub&gt;DDC1&lt;/sub&gt;</td>
<td>Stability Capacitor X7R Ceramic or Tantalum</td>
<td>4.7 uF – 10 uF</td>
</tr>
<tr>
<td>C&lt;sub&gt;DDC2&lt;/sub&gt;</td>
<td>X7R Ceramic</td>
<td>100 nF - 220 nF</td>
</tr>
</tbody>
</table>

3.4 Selecting the PNP external ballast transistor.

The maximum VREG current capability [I<sub>VREGMAX</sub>] using a PNP External Ballast transistor [Q<sub>PNP</sub>], must be determined by the allowed maximum power of the device. The designer should consider that the maximum power dissipation of the transistor will depend mainly on the following factors:

- package type
- dissipation mounting pad area on the PCB
- ambient temperature

Like maximum power supply potentials, maximum junction temperature is a worst case limitation which shouldn’t be exceeded. This is a critical point, since the lifetime of all semiconductors is inversely related to their operating junction temperature. For almost all transistors packages, the maximum power dissipation is specified to +25°C; and above this temperature, the power derates to the maximum Junction Temperature (+150°C). The R<sub>thJA</sub> depends considerably of the package transistor and the mounting pad...
area. The final product thermal limits should be tested and quantified in order to ensure acceptable performance and reliability.

The maximum power dissipation $P_{WR, MAX}$ by the device is given by:

$$ P_{WR, MAX} = \frac{T_{J, MAX} - T_{AMB}}{R_{th, JA}} $$

where $T_{AMB}$ is ambient temperature, $T_{J, MAX}$ is maximum junction temperature and $R_{th, JA}$ is the junction to Ambient Thermal Resistance of the Ballast transistor mounted on the specific PCB.

### 3.4.1 Static thermal analysis

It is extremely important to consider the derating of the power device above of $+25^\circ C$ (typical value for transistors). This guarantees that the junction temperature will be lower than the maximum operating junction temperature allowed by the device supplier. The following static thermal analysis using PSPICE Simulator demonstrates how the maximum power dissipation and the maximum supply current can be estimated for different voltage levels of VDDX.

**NOTE**

The data used in the next examples are fictional and should not be taken as specifications for particular systems. For specific calculations, please refer to the device datasheet.
Example analysis:

**Static Thermal Analysis**

![Static Thermal Analysis Diagram]

As a result of these examples, the maximum power dissipation of the ballast transistor is 780.312 mW. At this value, the transistor will reach its maximum operating temperature rating of 150°C. Therefore, the transistor can provide a maximum of 85.280 mA.

### 3.4.2 Recommended ballast transistors

Transistor specifications give the minimum and maximum gain. The worst case is usually significantly lower than the nominal figure on the transistor datasheet cover page. Furthermore, the datasheet values are usually given at room temperature (+25°C). The required gain should be calculated at cold temperature, because a PNP/NPN transistor has minimum gain at low temperature. The worst case gain at cold temperature can be obtained from the transistor supplier or can be estimated using the graphs given in the transistor datasheet.

**Table 4. Recommended Ballast transistor**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package Type</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCP53</td>
<td>SOT-223</td>
<td>NXP</td>
</tr>
<tr>
<td>PBSS5360PAS</td>
<td>DFN2020D-3 [SOT1061D]</td>
<td>NXP</td>
</tr>
</tbody>
</table>

The designer must follow and verify all layout/soldering footprint recommendations of the transistor supplier in order to reach a good performance transistor.

Make sure that the traces for decoupling capacitors are as short as possible. Shortening the capacitor traces to/from the ground/power plane is the most important concern for making a low inductance connection. In order to implement an appropriate decoupling for applications with LIN, CAN, SPI and IIC interfaces, consider the pairing of the power and ground planes close to each other (less than 10 mils). This creates an effect interplane capacitance, greatly reduces noise and increases power supply stability at the pins because of the extremely low inductance of this kind of capacitance in the layers. The number of discrete
capacitance can be reduced because the effective capacitors are greatly increased and the impedance of the power distribution network is reduced across a very broad frequency range.

4 Programming interface

4.1 BKGD

The background debug controller (BDC) is a single-wire, background debug system implemented in on chip hardware for minimal CPU intervention. The device BKGD pin interfaces directly to the BDC. The S12ZVC maintains the standard S12 serial interface protocol but introduces an enhanced handshake protocol and enhanced BDC command set to support the linear instruction set family of S12Z devices and offer easier, more flexible internal resource access over the BDC serial interface. The BKGD signal is used as a pseudo-open-drain signal for the background debug communication. The BKGD signal has an internal pull-up device.

![Diagram of Debug Connector Configuration](image)

4.2 Reset

The RESET signal is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The RESET pin has an internal pull-up device.

Upon detection of any reset source, an internal circuit drives the RESET pin low for 512 PLLCLK cycles. After 512 PLLCLK cycles the RESET pin is released. The internal reset of the MCU remains asserted while the reset generator completes the 768 PLLCLK cycles long reset sequence. In case the RESET pin is externally driven low for more than these 768 PLLCLK cycles (External Reset), the internal reset remains asserted longer.
In prototype designs, it is common to add a push-button to manually force a reset. In this case, the designer could choose to add a debounce capacitor to this button. In the event of an internal reset event, the MCU forces the RESET pin low and up again so that other circuits connected to this pin are reset as well. This reset pulse must last less than 24 μs. The debounce capacitance on the reset line must ensure that this timing constraint is met. Capacitors smaller than 330 pF are recommended.

**Figure 8. RESET Circuit**

### 4.3 TEST pin

This pin should always be grounded in all applications.
5 Clock circuitry

The S12ZVC devices have an internal 1 MHz internal RC oscillator with +/-1.3% accuracy over rated temperature range. There is an alternative to add an external resonator or crystal, for higher and tighter tolerance frequencies. The S12ZVC includes an oscillator control module capable of supporting either Loop Controlled Pierce (LCP) or Full Swing Pierce (FSP) oscillator configurations. The oscillation mode is selectable by software.

5.1 EXTAL and XTAL

These pins provide the interface for a crystal to control the internal clock generator circuitry. EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. If XOSCLCP is enabled, the MCU internal OSCCLK_LCP is derived from the EXTAL input frequency. If OSCE=0, the EXTAL pin is pulled down by an internal resistor of approximately 200 kΩ and the XTAL pin is pulled down by an internal resistor of approximately 700 kΩ.

The Pierce oscillator provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical crystal oscillators. S12ZVC supports crystals or resonators from 4MHz to 20MHz. The Input Capacitance of the EXTAL, XTAL pins is 7 pF.

![Reference oscillator circuit](image)

Table 5. Components of the oscillator circuit

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS</td>
<td>Bias Resistor</td>
</tr>
<tr>
<td>X1</td>
<td>Quartz Crystal / Ceramic Resonator</td>
</tr>
<tr>
<td>C1</td>
<td>Stabilizing Capacitor</td>
</tr>
<tr>
<td>C2</td>
<td>Stabilizing Capacitor</td>
</tr>
</tbody>
</table>

The load capacitors are dependent on the specifications of the crystal and on the board capacitance. It is recommended to have the crystal manufacturer evaluate the crystal on the PCB.
5.2 Suggestions for the PCB layout of oscillator circuit.

The crystal oscillator is an analog circuit and must be designed carefully and according to analog-board layout rules:

- External feedback resistor \([R_f]\) is not needed because it’s already integrated.
- It is recommended to send the PCB to the crystal manufacturer to determine the negative oscillation margin as well as the optimum regarding \(C_1\) and \(C_2\) capacitors. The data sheet includes recommendations for the tank capacitors \(C_1\) and \(C_2\). These values together with the expected PCB, pin, etc. stray capacity values should be used as a starting point.
- Signal traces between the S12ZVC pins, the crystal and, the external capacitors must be as short as possible, without using any via. This minimizes parasitic capacitance and sensitivity to crosstalk and EMI. The capacitance of the signal traces must be considered when dimensioning the load capacitors.
- Guard the crystal traces with ground traces (guard ring). This ground guard ring must be clean guard. This means that no current from and to other devices should be flowing through the guard ring. This guard ring should be connected to VSS of the S12ZVC with a short trace. Never connect the ground guard ring to any other ground signal on the board. Also avoid implementing ground loops.
- The main oscillation loop current is flowing between the crystal and the load capacitors. This signal path (crystal to \(C_{\text{EXTAL}}\) to \(C_{\text{XTAL}}\) to crystal) should be kept as short as possible and should have a symmetric layout. Hence, both capacitors’ ground connections should always be as close together as possible.

The following Figure 10, shows the recommended placement and routing for the oscillator layout.

![Figure 10. Suggested Crystal Oscillator Layout.](image)

6 High voltage inputs (HVI)

The high-voltage input (HVI) on port L has the following features:

- Input voltage proof up to \(V_{\text{HVI}}\)
- Digital input function with pin interrupt and wakeup from stop capability
- Analog input function with selectable divider ratio routable to ADC channel. Optional direct input bypassing voltage divider and impedance converter. Capable to wake-up from stop (pin interrupts in run mode not available). Open input detection.

The connection of an external pull device on a high-voltage input can be validated by using the built-in pull functionality of the HVI. Depending on the application type, an external pull down circuit can be detected with the internal pull-up device whereas an external pull-up circuit can be detected with the internal pull down device which is part of the input voltage divider.

Note that the following procedures make use of a function that overrides the automatic disable mechanism of the digital input buffer when using the HVI in analog mode. Make sure to switch off the override function when using the HVI in analog mode after the check has been completed.

### 6.1 External pulldown device

![Figure 11. Digital input read with Pull-up enabled](image)

### 6.2 External pull up device

![Figure 12. Digital input read with Pull-down enabled](image)
7 High current GPIO.

PP0, PP4, PP5 & PP6 supports 25 mA driver strength to VSS and PP2 supports 20 mA driver strength from VDDX (EVDD). These high current GPIOs cannot drive inductive/capacitive loads.

![High current GPIOs](image)

An external resistor REXT_HVI must be always connected to the high-voltage inputs to protect the device pins from fast transients and to achieve the specified pin input divider ratios when using the HVI in analog mode.

8 Inter-Integrated Circuit IIC

The inter-IC bus (IIC) is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange between devices. Being a two-wire device, the IIC bus minimizes the need for large numbers of connections between devices, and eliminates the need for an address decoder.

This bus is suitable for applications requiring occasional communications over a short distance between a number of devices. It also provides flexibility, allowing additional devices to be connected to the bus for further expansion and system development.

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Figure 14). When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open collector in order to perform the wired-AND function.

The interface is designed to operate up to 100 kbps with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF.
Figure 14. Connection of I2C-bus devices to the I2C-bus

Figure 15. Maximum value of RP as a function of bus capacitance for a standard-mode I2C-bus LIN Physical Layer
9 SENT transmitter interface

The Single Edge Nibble Transmission (SENT) module (SENTTX) is a transmitter for serial data frames which are implemented using the SENT encoding scheme. This module is based on the SAE J2716 information report titled “SENT - Single Edge Nibble Transmission for Automotive Applications” and released on January 27, 2010 (http://www.sae.org), April, 2007, and February, 2008. As per this standard, the SENT protocol is intended for use in applications where high resolution sensor data needs to be communicated from a sensor to an Engine Control Unit (ECU). It is intended as a replacement for the lower resolution methods of 10-bit A/Ds and PWM and as a simpler low-cost alternative to CAN or LIN.

The SENT encoding scheme is a unidirectional communications scheme from the sensor/transmitting device to the controller/receiving device which does not include a coordination signal from the controller/receiving device. The sensor signal is transmitted as a series of pulses with data encoded as falling to falling edge periods.

9.1 SENT/SPC physical layer

The receiver side (ECU) provides the stabilized 5 V voltage to supply the sensor. The communication line is pulled up by the 10 ÷ 51 kΩ resistor to the supply voltage. The receiver input is formed by the parasitic capacitance of the input pin and its ESD protection, and the 560 Ω / 2.2 nF EMC low-pass filter to suppress RF noise coupled to the communication line. The open-drain output pin on the MCU pulls down the communication line to generate the master trigger pulse. The transmitter provides a bidirectional open-drain I/O pin with an EMC filter to suppress the RF noise coupled to the communication line. The communication line is pulled down by its output driver to generate the SENT pulse sequence. Signal shaping is required to limit the radiated emissions. The maximum limits for the falling and rising edge durations are TFALL = 6.5 μs and TRISE = 18 μs with a maximum allowed 0.1 μs falling edge jitter. An example of a TLE4998C SENT/SPC compatible Hall sensor waveform is shown in Figure 16. The overall resistance of all connectors is limited to 1 Ω, the bus wiring to 0.1 nF/m capacitance and the maximum cable length to 5 m. The transmitter-receiver network devices are protected from short to ground and short-to-supply conditions. Upon recovery from these faults, normal operation is resumed.

Figure 16. SENT/SPC Circuit Topology
10 CAN physical Layer

The physical layer characteristics for CAN are specified in ISO-11898-2. This standard specifies the use of cable comprising parallel wires with an impedance of nominally 120 Ω (95 Ω as minimum and 140 Ω as maximum). The use of shielded twisted pair cables is generally necessary for electromagnetic compatibility (EMC) reasons, although ISO-11898-2 also allows for unshielded cable. A maximum line length of 40 meters is specified for CAN at a data rate of 1 Mb. However, at lower data rates, potentially much longer lines are possible. ISO-11898-2 specifies a line topology, with individual nodes connected using short stubs.

Though not exclusively intended for automotive applications, CAN protocol is designed to meet the specific requirements of a vehicle serial data bus: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth.

Each CAN station is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective stations. A typical CAN system with an S12Z microcontroller is shown in Figure 17.

![Figure 17. CAN System](image)

The S12ZVC family has a version with an on-chip CAN physical transceiver and a dedicated power supply using an external ballast transistor. Having these modules on-chip helps reduce the total amount of components required to implement CAN communication.

Like most others CAN physical transceivers, the CANH, CANL and SPLIT pins are available for the designer to terminate bus depending on the application. The Figure 18 and Figure 19 and show examples of the CAN node terminations.
Figure 18. CAN Physical transceiver circuit

Figure 19. CAN Physical transceiver circuit with common mode choke
## 10.1 CAN Components Data

### Table 6. CAN components

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Denotes a guard track next to a high/medium speed track. Guard tracks are connected such that each end of the track is connected to ground. A guard track should be connected to the ground plane at least every 500 mils. Spacing from any protected conductor and the guard track must not exceed 20 mils.</td>
</tr>
<tr>
<td>CBUS1 and CBUS2</td>
<td>The Capacitors CBUS1 and CBUS2 are not specifically required. They may be added for EMC reasons, in which case the maximum capacitance from either bus wire to ground must not exceed 300pF total. If zener stacks are also needed, the parasitic capacitance of the zener stacks must also be included in the total capacitance budget.</td>
</tr>
<tr>
<td>Z1 and Z2</td>
<td>The zener stacks Z1 and Z2 could be required to satisfy Automotive EMC requirements (ESD in particular). These devices should be placed close to the connector.</td>
</tr>
<tr>
<td>RTERM1, RTERM2 and CCOM1</td>
<td>Depending on the position of the node within the CAN network it might need a specific termination. ( \text{RTERM1, RTERM2 and CCOM1} ) must be that they assist in having an overall cable impedance. On a bus implementation of a CAN network only the two nodes on the two ends of the bus have terminator resistors. The nodes not placed on the end of the CAN bus do not have termination. A thorough analysis is required to maintain this requirement of the CAN networks. The SPLIT pin on the transceiver is optional and the designer might choose not to use it. This pin helps stabilize the recessive state of the CAN bus and can be enabled or disabled by software when required.</td>
</tr>
<tr>
<td>LBUS1 – Common mode choke</td>
<td>A common node choke on the CANH and CANL lines can help reduce coupled electromagnetic interference and needed to satisfy Automotive EMC requirements. This choke, together with transient suppressors on the transceiver pins can greatly reduce coupled electromagnetic noise, and high-frequency transients. LBUS1 is not specifically required</td>
</tr>
</tbody>
</table>

### 10.1.1 CAN Termination

In a transmission line, there are two current paths, one to carry the currents from the driver to the receiver and another to provide the return path back to the driver. In the CAN transmission lines is more complex because there are two signals that are sharing a common termination as well as a ground return path. For reliable CAN communications, it is essential that the reflections in the transmission line be kept as small as possible. This can only be done by proper cable termination. Figure 19 and Figure 20 demonstrates two CAN termination schemes.

Reflections happen very quickly during and just after signal transitions. On a long line, the reflections are more likely to continue long enough to cause the receiver to misread logic levels. On short lines, the reflections occur much sooner and have no effect on the received logic levels.
10.1.1.1 Parallel Termination

In CAN applications, both ends of the bus must be terminated because any node on the bus may transmit/receive data. Each end of the link has a termination resistor equal to the characteristic impedance of the cable, although the recommended value for the termination resistors is nominally 120 Ω (100 Ω as minimum and 130 Ω as maximum).

There should be no more than two terminating resistors in the network, regardless of how many nodes are connected, because additional terminations place extra load on the drivers. ISO-11898-2 recommends not integrating a terminating resistor into a node but rather attaching standalone termination resistors at the furthest ends of the bus. This is to avoid a loss of a termination resistor if a node containing that resistor is disconnected. The concept also applies to avoiding the connection of more than two termination resistors to the bus, or locating termination resistors at other points in the bus rather than at the two ends.

10.1.1.2 Parallel Termination with Common-Mode Filtering

To further enhance signal quality, split the terminating resistors at each end in two and place a filter capacitor, CSPLIT, between the two resistors. This filters unwanted high frequency noise from the bus lines and reduces common-mode emissions.
11 Unused pins

Unused digital pins can be left floating. To reduce power consumption, it is recommended that these unused digital pins are configured as inputs and have the internal pull resistor enabled. This will decrease current consumption and susceptibility to external electromagnetic noise. ADC unused pins should be grounded to reduce leakage currents. The EXTAL and XTAL pins default reset condition is to have pull-downs enabled. These pins should be connected to ground if not used.

The voltage regulator controller pin BCTL should be left unconnected if not used, and the VDDX voltage regulator must be configured to operate with the internal power transistor by setting the appropriate register (CPMUVREGCTRL register, bit EXTXON = 0, bit INTXON = 1). If the VDDC regulator is not used, the VDDC pin must be shorted with VDDX, and the BCTLC pin must be left unconnected.

12 General board layout guidelines

12.1 Traces recommendations

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing would be a round bend, as shown in the next Figure 22.

![Figure 22. Poor and Correct Way of Bending Traces in Right Angles.](image)

To minimize crosstalk, not only between two signals on one layer but also between adjacent layers, route them 90° to each other.

Complex boards need to use vias while routing; you have to be careful when using them. These add additional capacitance and inductance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length. While using differential signals, use vias in both traces or compensate the delay in the other trace.

12.2 Grounding

Grounding techniques apply to both multi-layer and single-layer PCBs. The objective of grounding techniques is to minimize the ground impedance and thus to reduce the potential of the ground loop from circuit back to the supply.

- Route high-speed signals above a solid and unbroken ground plane.
- Do not split the ground plane into separate planes for analog, digital, and power pins. A single and continuous ground plane is recommended.

- There should be no floating metal/shape of any kind near any area close to the microcontroller pins. Fill copper in the unused area of signal planes and connect these coppers to the ground plane through vias.

![Diagram of ground plane configurations](image)

**Figure 23. Eliminating floating metal/shape**
12.3 EMI/EMC and ESD Considerations for Layout

These considerations are important for all system and board designs. Though the theory behind this is well explained, each board and system experiences this in its own way. There are many PCB and component related variables involved.
This application note does not go into the electromagnetic theory or explain the whys of different techniques used to combat the effects, but it considers the effects and solutions most recommended as applied to CMOS circuits. EMI is radio frequency energy that interferes with the operation of an electronic device. This radio frequency energy can be produced by the device itself or by other devices nearby. Studying EMC for your system allows testing the ability of your system to operate successfully counteracting the effects of unplanned electromagnetic disturbances coming from the devices and systems around it. The electromagnetic noise or disturbances travels via two media: conduction and radiation.

The design considerations narrow down to:

- The radiated & conducted EMI from your board should be lower than the allowed levels by the standards you are following.
- The ability of your board to operate successfully counteracting the radiated & conducted electromagnetic energy (EMC) from other systems around it.

The EMI sources for a system consists of several components such as PCB, connectors, cables, etc. The PCB plays a major role in radiating the high frequency noise. At higher frequencies and fast-switching currents and voltages, the PCB traces become effective antennas radiating electromagnetic energy; e.g., a large loop of signal and corresponding ground. The five main sources of radiation are: digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of power and ground planes. Fast switching clocks, external buses, PWM signals are used as control outputs and in switching power supplies. The power supply is another major contributor to EMI. RF signals can propagate from one section of the board to another building up EMI. Switching power supplies radiate the energy which can fail the EMI test. This is a huge subject and there are many books, articles and white papers detailing the theory behind it and the design criteria to combat its effects.

Every board or system is different as far as EMI/EMC and ESD issues are concerned, requiring its own solution.

However, the common guidelines to reduce an unwanted generation of electromagnetic energy are as shown below:

- Ensure that the power supply is rated for the application and optimized with decoupling capacitors.
• Provide adequate filter capacitors on the power supply source. The bulk/bypass and decoupling capacitors should have low equivalent series inductance (ESL).

• Create ground planes if there are spaces available on the routing layers. Connect these ground areas to the ground plane with vias.

• Keep the current loops as small as possible. Add as many decoupling capacitors as possible. Always apply current return rules to reduce loop areas.

• Keep high-speed signals away from other signals and especially away from input and output ports or connectors.

13 References

• AN2727
• AN3208
• AN3335
• AN4219
• AN2536
• BasicThermalWP