Hardware Design Guidelines for S12ZVC
MagniV Mixed-Signal MCUs for CAN Applications

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1 Introduction

1.1 Purpose and scope

This document contains hardware guidelines for designing with the S12ZVC family of S12 MagniV Mixed-signal MCUs from Freescale. This includes:

• Device Overview S12ZVC Microcontroller
• Pin I/O overview
• Power Management
• RESET
• BKGD
• TEST Pin
• ADC Module
• DAC Module
• Analog Comparator
• High Voltage Input
• High and Low side Driver
• SENT Transmitter Interface

NOTE

Electrical parameters mentioned in this application note are subject to change in individual device specifications. Check each application against the latest data sheet for specific target devices.
2 S12ZVC device family overview

The MC9S12ZVC-Family is a new member of the S12 MagniV product line integrating a battery level (12 V) voltage regulator, supply voltage monitoring, high voltage inputs, and a CAN physical interface. It’s primarily targeted at CAN nodes like sensors, switch panels, or small actuators. It offers various low power modes and wakeup management to address state-of-the-art power consumption requirements.

Some members of the MC9S12ZVC-Family are also offered for high temperature applications requiring AEC-Q100 Grade 0 (-40°C to +150°C ambient operating temperature range). The MC9S12ZVC-Family is based on the enhanced performance, linear address space S12Z core and delivers an optimized solution with the integration of several key system components into a single device, optimizing system architecture, and achieving significant space savings.

2.1 MC9S12ZVC-Family comparison

Table 1 provides a summary of the MC9S12ZVC-Family. This information is intended to provide an understanding of the range of functionality offered by this microcontroller family.

<table>
<thead>
<tr>
<th>Feature</th>
<th>S12ZVCA 192</th>
<th>S12ZVCA 128</th>
<th>S12ZVC 96</th>
<th>S12ZVC 64</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package option</td>
<td>64-pin LQFP-EP</td>
<td>48-pin LQFP</td>
<td>64-pin LQFP-EP</td>
<td>48-pin LQFP</td>
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<tr>
<td>Core</td>
<td>S12Z</td>
<td>S12Z</td>
<td>S12Z</td>
<td>S12Z</td>
</tr>
<tr>
<td>Flash memory (ECC) [KByte]</td>
<td>192 128 96 64</td>
<td>192 128 96 64</td>
<td>192 128 96 64</td>
<td>192 128 96 64</td>
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<tr>
<td>EEPROM (ECC) [KByte] (4-byte erasable)</td>
<td>2 2 2 1</td>
<td>2 2 2 1</td>
<td>2 2 2 1</td>
<td>2 2 2 1</td>
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<tr>
<td>RAM (ECC) [KByte]</td>
<td>12 8 8 4</td>
<td>12 8 8 4</td>
<td>12 8 8 4</td>
<td>12 8 8 4</td>
</tr>
<tr>
<td>High Speed CAN Physical Layer</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>High Voltage Inputs</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
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<tr>
<td>Vreg for CAN PHY with ext. ballast (BCTLC)</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>VDDX/VSSX pins</td>
<td>2/2</td>
<td>2/2</td>
<td>2/2</td>
<td>2/2</td>
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<td>msCAN</td>
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<td>1</td>
<td>1</td>
<td>1</td>
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<tr>
<td>SCI</td>
<td>2</td>
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<td>2</td>
<td>1</td>
</tr>
<tr>
<td>SPI</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Feature</td>
<td>S12ZVCA</td>
<td>S12ZVCA</td>
<td>S12ZVC</td>
<td>S12ZVC</td>
</tr>
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<td>---------</td>
<td>---------</td>
<td>--------</td>
<td>--------</td>
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<td>192</td>
<td>128</td>
<td>96</td>
<td>64</td>
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<tr>
<td>IIC</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SENT (Transmitter)</td>
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<td>1</td>
<td>1</td>
<td>1</td>
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<tr>
<td>16-bit Timer channels</td>
<td>8</td>
<td>4</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>16-bit Timer channels (20 ns resolution(1))</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>16-bit PWM channels (20 ns resolution(1))</td>
<td>4</td>
<td>3</td>
<td>4</td>
<td>3</td>
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<tr>
<td>16-bit PWM channels</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
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<td>12-bit ADC channels</td>
<td>16</td>
<td>10</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>10-bit ADC channels</td>
<td>-</td>
<td>-</td>
<td>16</td>
<td>10</td>
</tr>
<tr>
<td>8-bit DAC</td>
<td>1</td>
<td>1</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>ACMP 5V (with rail-to-rail inputs)</td>
<td>2</td>
<td>2</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>EVDD (20 mA source)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Open Drain (5V GPIOs with disabled (PMOS))</td>
<td>10</td>
<td>5</td>
<td>10</td>
<td>5</td>
</tr>
<tr>
<td>N-GPIO (25mA sink)</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>General purpose I/O</td>
<td>42</td>
<td>28</td>
<td>42</td>
<td>28</td>
</tr>
</tbody>
</table>

1. at 25 MHz bus frequency
2.2 MC9S12ZVC-Family block diagram

Figure 1. High-level block diagram of the MC9S12ZVC-Family
3 Power management

3.1 Power supply pins

The power and ground pins are described in subsequent sections. Use bypass capacitors with low inductance characteristics and place them as close to the MCU as possible to account for fast signal transitions, which place high but short-duration current demands on the power supply.

NOTE
All ground pins must be connected together in the application.

3.1.1 VSUP—Voltage supply pin

VSUP is the 12 V supply voltage pin for the on chip voltage regulator. This is the voltage supply input from which the voltage regulator generates the on chip voltage supplies. It must be protected externally against a reverse battery connection.

![VSUP input diagram]

3.1.2 VDDX1, VDDX2, VSSX1, VSSX2—Digital I/O power and ground pins

VDDX is the voltage regulator output for the digital I/O drivers. It supplies the VDDX domain pads. The VSSX1 and VSSX2 pin is the ground pin for the digital I/O drivers. Bypass capacitor requirements on VDDX/VSSX depend on how heavily the MCU pins are loaded.

3.1.3 VDDA, VSSA—Power supply pins for ADC

These are the power supply and ground pins for the analog-to-digital converter and the voltage regulator. These pins must be externally connected to the voltage regulator (VDDX, VSSX). A separate bypass capacitor for the ADC supply is recommended.
3.1.4 VDDC

This is connected to the output voltage of the external bipolar. It is the feedback pin to the MCU also. When VDDC is not used, it must be shorted with VDDX and the user must keep the EXTCON in CPMUVREGCTL enabled.

3.2 PNP external ballast transistor

3.2.1 Base Control Pins for external PNP

- **BCTL** - Base Control Pin for external PNP: BCTL is the ballast connection for the on chip voltage regulator. It provides the base current of an external BJT (PNP) of the VDDX and VDDA supplies. An additional 1 KΩ resistor between emitter and base of the BJT is required.
- **BCTLC** - Base Control Pin for external PNP for VDDC: BCTLC is the ballast connection for the on chip CAN voltage regulator. It provides the base current of an external BJT.
Figure 4. External PNP ballast transistor for VDDX

Figure 5. External PNP ballast transistor for VDDC

Table 3. PowerVDDX and VDDC

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDX</td>
<td>QPNPX</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>R&lt;sub&gt;BCTLX&lt;/sub&gt;</td>
<td>1</td>
<td>kΩ</td>
</tr>
<tr>
<td></td>
<td>C&lt;sub&gt;BCTL1&lt;/sub&gt; X7R Ceramic</td>
<td>100 to 220</td>
<td>nF</td>
</tr>
<tr>
<td></td>
<td>C&lt;sub&gt;PNPX1&lt;/sub&gt; X7R Ceramic or Tantalum</td>
<td>4.7 to 10</td>
<td>uF</td>
</tr>
<tr>
<td></td>
<td>C&lt;sub&gt;PNPX2&lt;/sub&gt; X7R Ceramic</td>
<td>100 to 220</td>
<td>nF</td>
</tr>
<tr>
<td>VDDC</td>
<td>QPNPC</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>R&lt;sub&gt;BCTL2&lt;/sub&gt;</td>
<td>1</td>
<td>kΩ</td>
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<tr>
<td></td>
<td>C&lt;sub&gt;BCTL&lt;/sub&gt; X7R Ceramic</td>
<td>100 to 220</td>
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<td></td>
<td>C&lt;sub&gt;PNPC1&lt;/sub&gt; X7R Ceramic or Tantalum</td>
<td>4.7 to 10</td>
<td>uF</td>
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<tr>
<td></td>
<td>C&lt;sub&gt;PNPC2&lt;/sub&gt; X7R Ceramic</td>
<td>100 to 220</td>
<td>nF</td>
</tr>
</tbody>
</table>
The maximum VREG current capability [IVREGMAX] using a PNP External Ballast transistor [QPNP], must be determinated by the allowed maximum power of the device. The designer should to consider that the maximum power dissipation of the transistor will depend mainly on the following factors:

- Current demand
- Package type
- Dissipation mounting pad area on the PCB
- Ambient temperature

Like maximum power supply potentials, maximum junction temperature is a worst case limitation which shouldn’t be exceeded. This is a critical point, since the lifetime of all semiconductors is inversely related to their operating junction temperature. For almost all transistors packages, the maximum power dissipation is specified to +25°C; and above this temperature, the POWER derates to the maximum Junction Temperature (+150°C). The $R_{thJA}$ depends considerably of the package transistor and the mounting pad area. The final product thermal limits should be tested and quantified in order to insure acceptable performance and reliability.

![Diagram showing maximum power dissipation versus temperature](image)

**Figure 6. Maximum power dissipation versus temperature**

The maximum power dissipation $PWR_{MAX}$ by the device is given by:

$$ PWR_{MAX} = \frac{T_{J\text{MAX}} - T_{AMB}}{R_{thJA}} $$

where $T_{AMB}$ is ambient temperature, $T_{J\text{MAX}}$ is maximum junction temperature and $R_{thJA}$ is the Junction to Ambient Thermal Resistance of the Ballast transistor mounted on the specific PCB.

### 3.2.2 Static thermal analysis

It is extremely important to consider the derating of the power device above of +25°C (typical value for transistors). This guarantees that the maximum junction temperature will be lower than the maximum storage temperature. The following static thermal analysis using PSPICE Simulator demonstrates how chip junction temperature and the maximum power dissipation can be estimated.

Assuming:
VSUP<sub>MAX</sub> = 14V  
VDDD<sub>MAX</sub> = 5.15 V  
VDDD<sub>MIN</sub> = 4.58 V  
TAMB<sub>MAX</sub> = +85°C  
TJ<sub>MAX</sub> = +150°C  
Rth<sub>JA</sub> = 83.3 °C/W

Static Thermal Analysis

![Diagram of Static Thermal Analysis]

As a result, the maximum power dissipation of the ballast transistor is 780.312 mW, this value reaches the maximum storage temperature of the device, +150°C; and therefore the device can provide 85.280 mA as the maximum VREG current capability.

3.2.3 Recommended ballast transistors

Transistor specifications give the minimum and maximum gain. The worst case is usually significantly lower than the nominal figure on the transistor datasheet cover page. Furthermore, the datasheet values are usually given at room temperature (+25 °C). The required gain should be calculated at cold temperature, because a PNP/NPN transistor has minimum gain at low temperature. The worst case gain at cold temperature can be obtained from the transistor supplier or can be estimated using the graphs given in the transistor datasheet.
### Table 4. Recommended ballast transistors

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package Type</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCP53 (Actually used in the EVB)</td>
<td>SOT-223</td>
<td>ONSEMI/NXP/FAIRCHILD/ZETEX</td>
</tr>
<tr>
<td>2SB1260 / 2SB1181</td>
<td>SOT-89</td>
<td>ROHM</td>
</tr>
<tr>
<td>2SA1952 TBV</td>
<td>DPAK</td>
<td>ROHM</td>
</tr>
<tr>
<td>2SB1181 TBV</td>
<td>SOT-89</td>
<td>ROHM</td>
</tr>
<tr>
<td>MJD32 TBV</td>
<td>DPAK</td>
<td>ONSEMI/FAIRCHILD</td>
</tr>
<tr>
<td>MJD45H11 TBV</td>
<td>DPAK</td>
<td>ONSEMI/FAIRCHILD</td>
</tr>
</tbody>
</table>

The designer must follow and verify all Layout/soldering footprint recommendations of the transistor supplier in order to reach a good performance transistor.

### 3.3 Decoupling/Bypass capacitors

Make sure that the traces for decoupling capacitors are as short as possible. Shortening the capacitor traces to/from the ground/power plane is the most important concern for making a low inductance connection.

For tantalum and electrolytic capacitors, the designer must be sure to select a high enough voltage to take account the derating over time. It is to pick a voltage at least 2x higher than the voltage being applied to the capacitor. The derating curve can be found in the data sheet of the capacitor and that the voltage capacitor selected is enough.

The designer must take care that the bulk/bypass capacitance does not throw the power rail out of the correct power-up or power-down sequence (the order of power supplies starting-up and powering-down). In order to implement an appropriate decoupling for applications with LIN, CAN, SPI, and IIC interfaces, pairing of the power and ground planes close to each other must be considered (<10 mils). This creates an effect interplane capacitance, greatly reduces noise, and increases power supply stability at the pins because of the extremely low inductance of this kind of capacitance in the layers. The number of discrete capacitors can be reduced because the effective capacitance is greatly increased and the impedance of the power distribution network is reduced across a very broad frequency range.

### 4. RESET

The RESET signal is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state and an output when an internal MCU function causes a reset. When the MCU initiates a reset sequence due to a COP (Watchdog Timeout) or clock monitor reset, it is important that the line is not externally pulled low for more than 768 cycles. This is because the reset circuitry within the MCU uses the reset pull time as a way to detect the reset source. If the reset line is held low more...
than 768 cycles, the MCU would detect the reset as an external PIN reset, instead of the appropriate source of the event (COP or Clock Monitor).

The reset sequence is 768 cycles long. During this time, the PLLCLK is running with the frequency fVCORST. This frequency is specified to be between 8 MHz and 32 MHz. Therefore, the fastest reset sequence would be 768 cycles @ 32 MHz = 24 µs. The longest reset sequence would be 768 cycles @ 8 MHz = 96 µs. If the reset line has a push button to manually force a reset, the designer could choose to add a debounce capacitor to this button. The debounce capacitance must be such that the time it takes for the reset line to go down and up again, in the event of an internal reset, is less than 768 cycles (24 µs to 96 µs), so it can only support a capacitor value of a couple pF. If the designer wished to add a larger debounce capacitor, a diode is required between the reset pin on the MCU and the button as shown in Figure 8.

The RESET pin has an internal pull-up device.

![Figure 8. RESET circuit](image)

5 Programming circuit

The S12ZVC family is programmed via the BDM protocol. All the S08 and S12 microcontrollers of Freescale use this protocol and many third party tools are able to program via BDM. The standard BDM connector is a 2 by 3 pin header with 100 mil pitch. Figure 9 describes the BDM connector pinout.

The BDM protocol is a serial protocol that is transmitted through the BKGD line. This line comes with an internal weak pull-up resistor so, it requires an external strong pull up resistor in the range of 4.7k to 10k ohm. If a filter capacitor is desired, bear in mind that the BKGD pin is used to serially program the microcontroller so high capacitances can affect the slew-rate of the signals being transmitted and prevent correct programming. 10 pF ceramic capacitors have been tested successfully although they are not necessary. The BDM connector requires connection to the RESET pin, voltage (VDDX), and ground. It is recommended to add a ceramic capacitor to VDDX near the connector to reduce noise that could be injected by the programming circuitry to the power supply. A capacitor from 10 nF to 100 nF X7R is recommended.
5.1 BKGD

The background debug controller (BDC) is a single-wire, background debug system implemented in on chip hardware for minimal CPU intervention. The device BKGD pin interfaces directly to the BDC.

The S12ZVC maintains the standard S12 serial interface protocol but introduces an enhanced handshake protocol and enhanced BDC command set to support the linear instruction set family of S12Z devices and offer easier, more flexible internal resource access over the BDC serial interface.

The BKGD signal is used as a pseudo-open-drain signal for the background debug communication. The BKGD signal has an internal pull-up device.

![Figure 9. Debug connector configuration](image)

6 External and internal RC oscillator

The S12ZVC devices have an internal 1 MHz internal RC oscillator with +/-1.3% accuracy over rated temperature range. There is an alternative to add an external resonator or crystal for higher and tighter tolerance frequencies. The S12ZVC includes an oscillator control module capable of supporting either Loop Controlled Pierce (LCP) or Full Swing Pierce (FSP) oscillator configurations. The oscillation mode is selectable by software.

6.1 EXTAL and XTAL

These pins provide the interface for a crystal to control the internal clock generator circuitry. EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. If XOSCLCP is enabled, the MCU internal OSCCLK_LCP is derived from the EXTAL input frequency. If OSCE=0, the EXTAL pin is pulled down by an internal resistor of approximately 200 kΩ and the XTAL pin is pulled down by an internal resistor of approximately 700 kΩ.

The Pierce oscillator provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical crystal oscillators. S12ZVC supports crystals or resonators from 4 MHz to 20 MHz. The Input Capacitance of the EXTAL, XTAL pins is 7 pF.
The load capacitors are dependent on the specifications of the crystal and on the board capacitance. It is recommended to have the crystal manufacturer evaluate the crystal on the PCB.

### 6.2 Suggestion for the PCB layout of oscillator circuit

The crystal oscillator is an analog circuit and must be designed carefully and according to analog-board layout rules:

- Signal traces between the S12ZVC pins, the crystal, and the external capacitors must be as short as possible, **without using any vias**. This minimizes parasitic capacitance and sensitivity to crosstalk and EMI. The capacitance of the signal traces must be considered when dimensioning the load capacitors.

- Guard the crystal traces with ground traces (guard ring). This ground guard ring must be clean ground. This means that no current from and to other devices should be flowing through the guard ring. This guard ring should be connected to VSS of the S12ZVC with a short trace. Never connect the ground guard ring to any other ground signal on the board. Also, avoid implementing ground loops.

- The main oscillation loop current is flowing between the crystal and the load capacitors. This signal path (crystal to CEXITAL to CXTAL to crystal) should be kept as short as possible and should have a symmetric layout. Hence, both capacitors' ground connections should always be as close together as possible.

- With 2-layer boards, do not route any digital-signal lines on the opposite side of the PCB under the crystal area. In any case, it is a good design practice to fill the opposite side of the PCB with clean ground and also connect this ground to VSS of the S12ZVC.
The following figure shows the recommended placement and routing for the oscillator layout.

![Figure 11. Suggested crystal oscillator layout](image)

### 7 TEST pin

This pin should always be grounded in all applications.

![Figure 12. TEST pin connection](image)

### 8 DAC module

The DAC_8B5V module is a digital-to-analog converter. The converter works with a resolution of 8-bit and generates an output voltage between VRL and VRH. It is recommended to add a ceramic capacitor between VRH and VRL, close to the microcontroller.
The module consists of configuration registers and two analog functional units, a DAC resistor network, and an operational amplifier. The configuration registers provide all required control bits for the DAC resistor network and for the operational amplifier.

9 High Voltage Inputs (HVI)

The high-voltage input (HVI) on port L has the following features:

- Input voltage proof up to VHVI
- Digital input function with pin interrupt and wakeup from stop capability
- Analog input function with selectable divider ratio routable to ADC channel. Optional direct input bypassing voltage divider and impedance converter. Capable to wake up from stop (pin interrupts in run mode not available). Open input detection.
The connection of an external pull device on a high-voltage input can be validated by using the built-in pull functionality of the HVI. Depending on the application type, an external pull down circuit can be detected with the internal pull-up device whereas an external pull-up circuit can be detected with the internal pull down device which is part of the input voltage divider.

Note that the following procedures make use of a function that overrides the automatic disable mechanism of the digital input buffer when using the HVI in analog mode. Make sure to switch off the override function when using the HVI in analog mode after the check has been completed.

An external resistor REXT_HVI must be always connected to the high-voltage inputs to protect the device pins from fast transients and to achieve the specified pin input divider ratios when using the HVI in analog mode.

### 9.1 External pulldown device

![Diagram of External Pulldown Device]

**Figure 15. Digital Input Read with pullup enabled**
9.2 External pull-up device

Figure 16. Digital Input Read with pulldown enabled

10 High current GPIO

PP0, PP4, PP5, and PP6 support 25 mA driver strength to VSS and PP2 supports 20 mA driver strength from VDDX (EVDD). These high current GPIOs cannot drive inductive/capacitive loads.

Figure 17. High current GPIO
11 Inter-Integrated Circuit (IIC)

The inter-IC bus (IIC) is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange between devices. Being a two-wire device, the IIC bus minimizes the need for large numbers of connections between devices and eliminates the need for an address decoder.

This bus is suitable for applications requiring occasional communications over a short distance between a number of devices. It also provides flexibility, allowing additional devices to be connected to the bus for further expansion and system development.

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Figure 18). When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function.

The interface is designed to operate up to 100 kbps with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF.

Figure 18. Connection of I2C-bus devices to the I2C-bus
The Single Edge Nibble Transmission (SENT) module (SENTTX) is a transmitter for serial data frames which are implemented using the SENT encoding scheme. This module is based on the SAE J2716 information report titled “SENT - Single Edge Nibble Transmission for Automotive Applications” and released on January 27, 2010 (http://www.sae.org), April, 2007, and February, 2008. As per this standard, the SENT protocol is intended for use in applications where high resolution sensor data needs to be communicated from a sensor to an Engine Control Unit (ECU). It is intended as a replacement for the lower resolution methods of 10-bit A/Ds and PWM and as a simpler low-cost alternative to CAN or LIN.

The SENT encoding scheme is a unidirectional communications scheme from the sensor/transmitting device to the controller/receiving device which does not include a coordination signal from the controller/receiving device. The sensor signal is transmitted as a series of pulses with data encoded as falling to falling edge periods.

12.1 SENT/SPC physical layer

The receiver side (ECU) provides the stabilized 5 V voltage to supply the sensor. The communication line is pulled up by the 10 ÷ 51kΩ resistor to the supply voltage. The receiver input is formed by the parasitic capacitance of the input pin and its ESD protection, and the 560 Ω / 2.2 nF EMC low-pass filter to suppress RF noise coupled to the communication line. The open-drain output pin on the MCU pulls down the communication line to generate the master trigger pulse.
The transmitter provides a bidirectional open-drain I/O pin with an EMC filter to suppress the RF noise coupled to the communication line. The communication line is pulled down by its output driver to generate the SENT pulse sequence.

Signal shaping is required to limit the radiated emissions. The maximum limits for the falling and rising edge durations are $T_{FALL} = 6.5 \ \mu s$ and $T_{RISE} = 18 \ \mu s$ with a maximum allowed 0.1 $\mu s$ falling edge jitter. An example of a TLE4998C SENT/SPC compatible Hall sensor waveform is shown in Figure 20.

The overall resistance of all connectors is limited to 1 $\Omega$, the bus wiring to 0.1 nF/m capacitance and the maximum cable length to 5 m. The transmitter-receiver network devices are protected from short-to-ground and short-to-supply conditions. Upon recovery from these faults, normal operation is resumed.

![Figure 20. SENT/SPC circuit topology](image)

13 CAN physical layer

The S12ZVC family has an on-chip CAN physical transceiver and a dedicated power supply using an external ballast transistor VDDC. Having these modules on-chip helps reduce the total amount of components required to implement CAN communication. As any other CAN physical transceiver, the CANH, CANL and SPLIT pins are available for the designer to terminate bus depending on the application. Figure 21 and Figure 22 show an example of CAN node terminations.
Figure 21. CAN physical transceiver circuit

Figure 22. CAN physical transceiver circuit with common mode choke
### Table 6. CAN physical layer

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Guard Track" /></td>
<td>Denotes a guard track next to a high/medium speed track. Guard tracks are connected such that each end of the track is connected to ground. A guard track should be connected to the ground plane at least every 500 mils. Spacing from any protected conductor and the guard track must not exceed 20 mils.</td>
</tr>
<tr>
<td>CBUS1 and CBUS2</td>
<td>The Capacitors CBUS1 and CBUS2 are not specifically required. They may be added for EMC reasons, in which case the maximum capacitance from either bus wire to ground must not exceed 300pF total. If zener stacks are also needed, the parasitic capacitance of the zener stacks must also be included in the total capacitance budget.</td>
</tr>
<tr>
<td>Z1 and Z2</td>
<td>The zener stacks Z1 and Z2 could be required to satisfy the Automotive EMC requirements (ESD in particular). These devices should be placed close to the connector.</td>
</tr>
<tr>
<td>RTERM1, RTERM2 and CCOM1</td>
<td>Depending on the position of the node within the CAN network it might need a specific termination. $R_{TERM1}$, $R_{TERM2}$, and $C_{COM1}$ must be such that they assist in having an overall cable impedance. On a bus implementation of a CAN network only the two nodes on the two ends of the bus have terminator resistors. The nodes not placed on the end of the CAN bus do not have termination. A thorough analysis is required to maintain this requirement of the CAN networks. The SPLIT pin on the transceiver is optional and the designer might choose not to use it. This pin helps stabilize the recessive state of the CAN bus and can be enabled or disabled by software when required.</td>
</tr>
<tr>
<td>LBUS1 – Common mode choke</td>
<td>A common node choke on the CANH and CANL lines can help reduce coupled electromagnetic interference and needed to satisfy Automotive EMC requirements. This choke, together with transient suppressors on the transceiver pins, can greatly reduce coupled electromagnetic noise and high-frequency transients.</td>
</tr>
</tbody>
</table>
14 General board layout guidelines

14.1 Dealing with two-layer board

If your project cannot afford the cost of a four-layer board, then for a two-layer board you need to use Multi-Point-ground. You need to make every effort to reduce coupled noise. Provide as much ground area as possible, instead of running several traces, use shorter and wider traces. As the (return) current always flows back to source, avoid large loops. They are quick to couple noise from the electromagnetic radiations. Separate high/medium-speed signals (e.g., clock signals) from PWM signals and digital from analog signals; the placement is important.

Figure 23. Layout considerations for two layers
Maximize cooper areas in order to provide a low impedance for power supply decoupling careful arrangement of components and connections (traces) may allow large areas of PCB to be filled with GROUND.

**Figure 24. Layout Considerations for GND plane of the microcontroller**

There should be no floating metal/shape of any kind near any area close to the microcontroller pins.
14.2 Traces recommendations

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing would be a round bend, as shown in figure below.

To minimize crosstalk, not only between two signals on one layer but also between adjacent layers, route them 90° to each other. Complex boards need to use vias while routing; you have to be careful
when using them. These add additional capacitance and inductance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length. While using differential signals, use vias in both traces or compensate the delay in the other trace.

### 14.3 EMI/EMC and ESD considerations for layout

These considerations are important for all system and board designs. Though the theory behind this is well explained, each board and system experiences this in its own way. There are many PCB and component related variables involved.

This application note does not go into the electromagnetic theory or explain the whys of different techniques used to combat the effects, but it considers the effects and solutions most recommended as applied to CMOS circuits. EMI is radio frequency energy that interferes with the operation of an electronic device. This radio frequency energy can be produced by the device itself or by other devices nearby. Studying EMC for your system allows testing the ability of your system to operate successfully, counteracting the effects of unplanned electromagnetic disturbances coming from the devices and systems around it. The electromagnetic noise or disturbances travels via two media: conduction and radiation.

**Figure 27. Electromagnetic noise propagation**

![Electromagnetic noise propagation diagram](image)

The design considerations narrow down to:

- The radiated and conducted EMI from your board should be lower than the allowed levels by the standards you are following.
- The ability of your board to operate successfully counteracting the radiated and conducted electromagnetic energy (EMC) from other systems around it.

The EMI sources for this system consists of several components such as PCB, connectors, cables, etc.

The PCB plays a major role in radiating the high frequency noise. At higher frequencies and fast-switching currents and voltages, the PCB traces become effective antennas radiating electromagnetic energy; e.g., a large loop of signal and corresponding ground. The five main sources of radiation are: digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of power and ground planes. Fast switching clocks, external buses, PWM signals are used as control outputs and in switching power supplies. The power
supply is another major contributor to EMI. RF signals can propagate from one section of the board to another building up EMI. Switching power supplies radiate the energy which can fail the EMI test.

This is a huge subject and there are many books, articles, and white papers detailing the theory behind it and the design criteria to combat its effects.

14.3.1 EMI

Every board or system is different as far as EMI/EMC issues are concerned, requiring its own solution. However, the common guidelines to reduce an unwanted generation of electromagnetic energy are as shown below:

- Use multiple decoupling capacitors with different values and appropriate power supply decoupling techniques. Be aware that every capacitor has a self-resonant frequency.
- Provide adequate filter capacitors on the power supply source. These capacitors and decoupling capacitors should have low equivalent series inductance (ESL).
- Create ground planes if there are spaces available on the routing layers. Connect these ground areas to the ground plane with vias.
- Keep the current loops as small as possible. Add as many decoupling capacitors as possible. Always apply current return rules to reduce loop areas.
- Keep high-speed signals away from other signals and especially away from input and output ports or connectors.
- Apply current return rules to connect the grounds together while isolating the ground plane for the analog portion. If the project does not use ADC and there are no analog circuits do not isolate grounds.
- Avoid connecting the ground splits with a ferrite bead. At high frequencies, a ferrite bead has high impedance and creates a large ground potential difference between the planes.

14.3.2 ESD

A supply voltage glitch or ESD will put the device in an unknown state. Therefore, it is important to have a good PCB layout for optimum noise and ESD performance. The similar ESD protection diodes can be utilized for LINphy pins as well. Keep the loop area of critical traces as short as possible. If your design needs to bring any pin like GPIO to a connector (for external connectivity) you need to take special ESD care by adding ESD protection parts.

15 References

16 Glossary

VBAT = Auto Battery Supply
VSUP = via diode against negative voltages protected VBAT supply
VSENSE = Voltage Sense Pin, commonly known as pin connected to VBAT
UHV = Ultra High Voltage
HVI = High Voltage Input
DAC = Digital to Analog Converter
VRL = Low Reference Voltage
VRH = High Reference Voltage
FVR = Full Voltage Range
SSC = Special Single Chip