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USB Hub Keyboard for the MC68HC08KH12

Designer Reference Manual

M68HC08
Microcontrollers

DRM015/D
Rev. 0.0, 3/2003

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USB Hub Keyboard for the MC68HC08KH12

Designer Reference Manual — Rev 0.0

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Section 1. System Overview

1.1 Introduction

This manual describes a reference design of a Universal Serial Bus Hub Keyboard for the MC68HC08KH12.

The Motorola MC68HC08KH12 (hereafter referred as KH12) is a member of the HC08 Family of microcontrollers (MCUs). The features of the KH12 include a USB hub controller and an embedded USB device, which makes this MCU suited for hub keyboards applications. The KH12 is available in 64-QFP and 52-TQFP packages. The 64-QFP device includes 4 down-stream ports while the 52-TQFP device includes only 2 down-stream ports. This reference design is demonstrated using the KH12 with 64-pin QFP device. The main features of the hub keyboard include:

- Configurable 1 – 4 downstream ports (only two downstream ports components were assembled in the demo board)
- Windows 98, ME and 2000 and XP compatible
- Power management keys (power, wake and sleep) support
- Multimedia keys support

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1.2 System Overview

The hub keyboard is a compound device containing a full-speed hub with optional 1–4 external downstream ports and an embedded USB keyboard. Figure 1-1 shows the block diagram of the system.

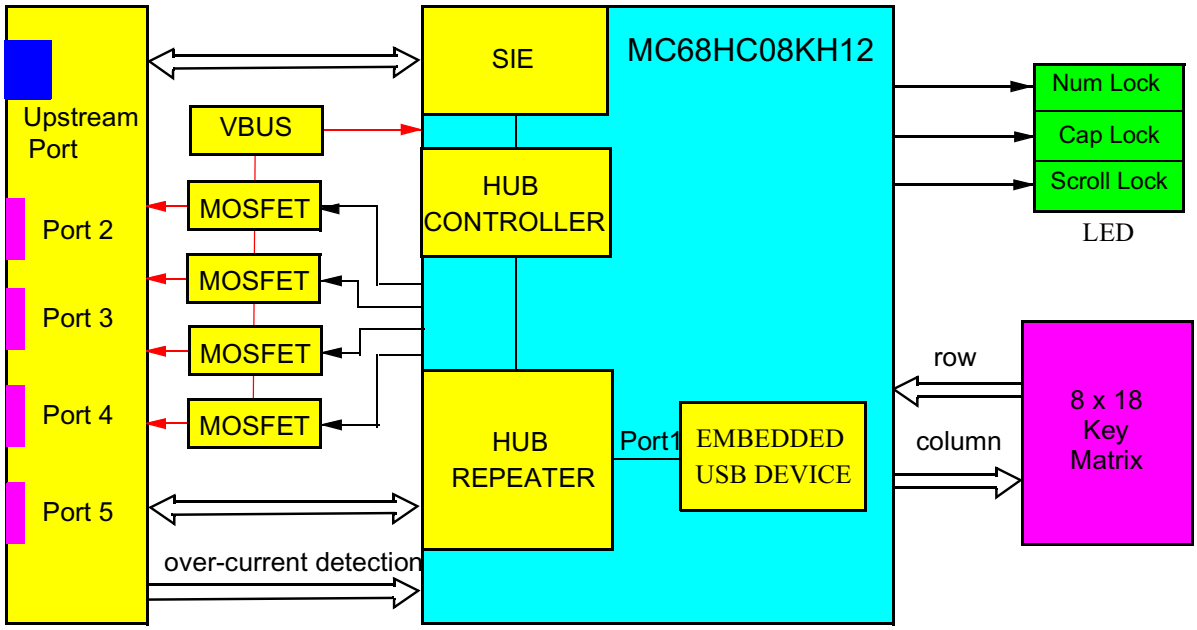

Figure 1-1. Block Diagram

1.2.1 Hub Function

The hub provides electrical interfaces between host and USB devices. It is compliant to the USB specification 1.1 and therefore supports both the full-speed and low-speed devices. Listed below are the major functions of the hub:

- Power Management
- Bus connectivity to USB devices
- Device connect and disconnect detection
- Bus fault detection and recovery

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System Overview

In KH12, there are four downstream ports named port 1 to port 4 and one embedded USB device treated as a device connected to port 5 of the hub. However such arrangements are inconvenience for configurations of different number of ports. Therefore the port numbers are re-mapped by firmware and named as logical ports. The host will only see the logical port numbers. After re-map, the embedded USB device is connected to port 1 and the external port numbers are from 2 to 5.

1.2.2 Keyboard Function

The keyboard is an embedded USB device. In system point of view it is an unremovable USB device connected to the downstream port 1 of the hub. Listed below are the major features of the keyboard:

- Power management keys (power, wake and sleep) support
- Multimedia keys support
- Function key support
- “000” key is implemented (one key strike, three “000” generated)

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Section 2. Hardware Overview

2.1 Hardware Description

The system consists major of a KH12, P-channel MOSFETs for bus-power control and poly-resistors for power protection.

2.1.1 CPU Bus Frequency

The clock generator module is optimized to generate a 48MHz reference for the USB module, from a 6MHz crystal. The CPU bus running at 6MHz with PLL turned on.

2.1.2 Hub Module

The hub consists of

- Control Endpoint 0 with separated 8 bytes of transmit and receive buffers
- Interrupt Endpoint 1 with 1 byte of transmit buffer

2.1.3 Embedded Device Module

The embedded device consists of

- Control Endpoint 0 with separated 8 bytes of transmit and receive buffers
- Interrupt Endpoint 1 and 2 with shared 8 bytes of transmit buffer

2.1.4 I/O Ports

The usage of different I/O ports are shown as below:

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- Port D, one of the three keyboard interrupt ports, is used as keyboard row for detecting key pressed and released
- Port A, port B, PTC4 and PTE4 are used for keyboard column scanning
- Port F is used for power control and over-current detection

2.1.5 Power Management

The power control of downstream ports are by turning the p-channel MOSFET on and off. Over-current protection is by means of the polyswitch. Over-current detection is by direct monitoring of the voltage levels of the downstream bus-power lines. PSW1 is active low and a logic zero turns on the MOSFET. C1 is used to turn off the MOSFET during KH12 starting up to reduce the inrush current.

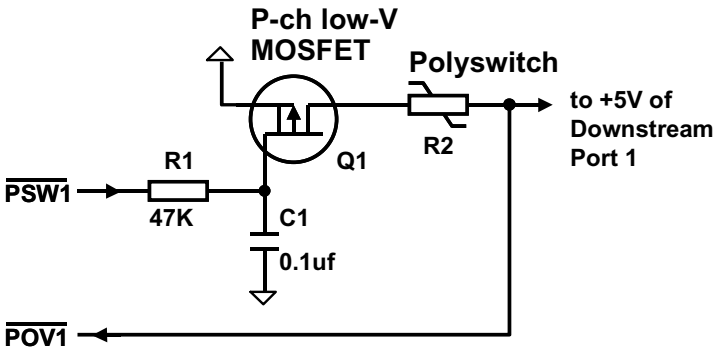

Figure 2-1. Power Management

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Section 3. Firmware Description

3.1 Firmware Structure

The firmware consists of five main parts:

- Hub functions routine
- Device functions routine
- Timer interrupt routine
- Hub interrupt and handler routine
- Device interrupt and handler routine

Figure 3-1 shows the flow of the main program and the interrupt routine. The main program calls the hub function routine and the device functions routine continuously. The program uses three interrupt functions including timer, hub and embedded device interrupts. The hub functions routine does the high level hub functions such as power management and device connect and disconnect detections. The device function routine does the high level keyboard function such as key matrix scanning and reporting. The timer interrupt routine resets the timer and sets the corresponding timer tick flags used for the main program as time references. The hub and device interrupt routines handles the USB low level hub and Human Interface Device protocols.

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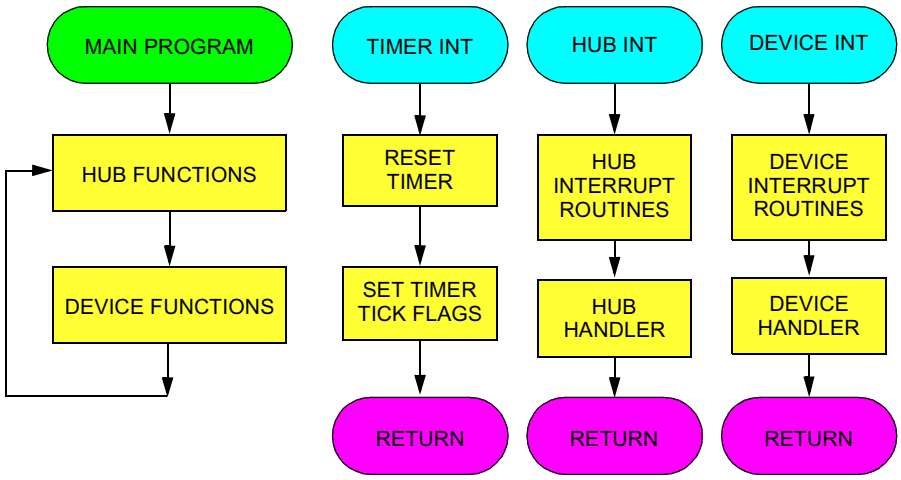

Figure 3-1. Firmware Structure

3.1.1 Hub Functions Routine

Figure 3-2 shows the hub functions routine. After initialization, it waits for host to configure the hub to configured stage. Before the hub is configured the only task of it is to enter suspend stage if the USB bus idles for more than 6ms. After the hub is configured, it enters configured stage and enable endpoint 1. The host will begin to issue commands to the hub to set power to all of the downstream ports one by one. After the host has set power to the embedded USB device, the hub reports downstream port 1 connected since the embedded device, keyboard, is an unremovable downstream port device, It continues to detects any changes in the downstream ports such as connect and disconnect and over-current. The hub reports any changes to the host through endpoint 1 if there are any.

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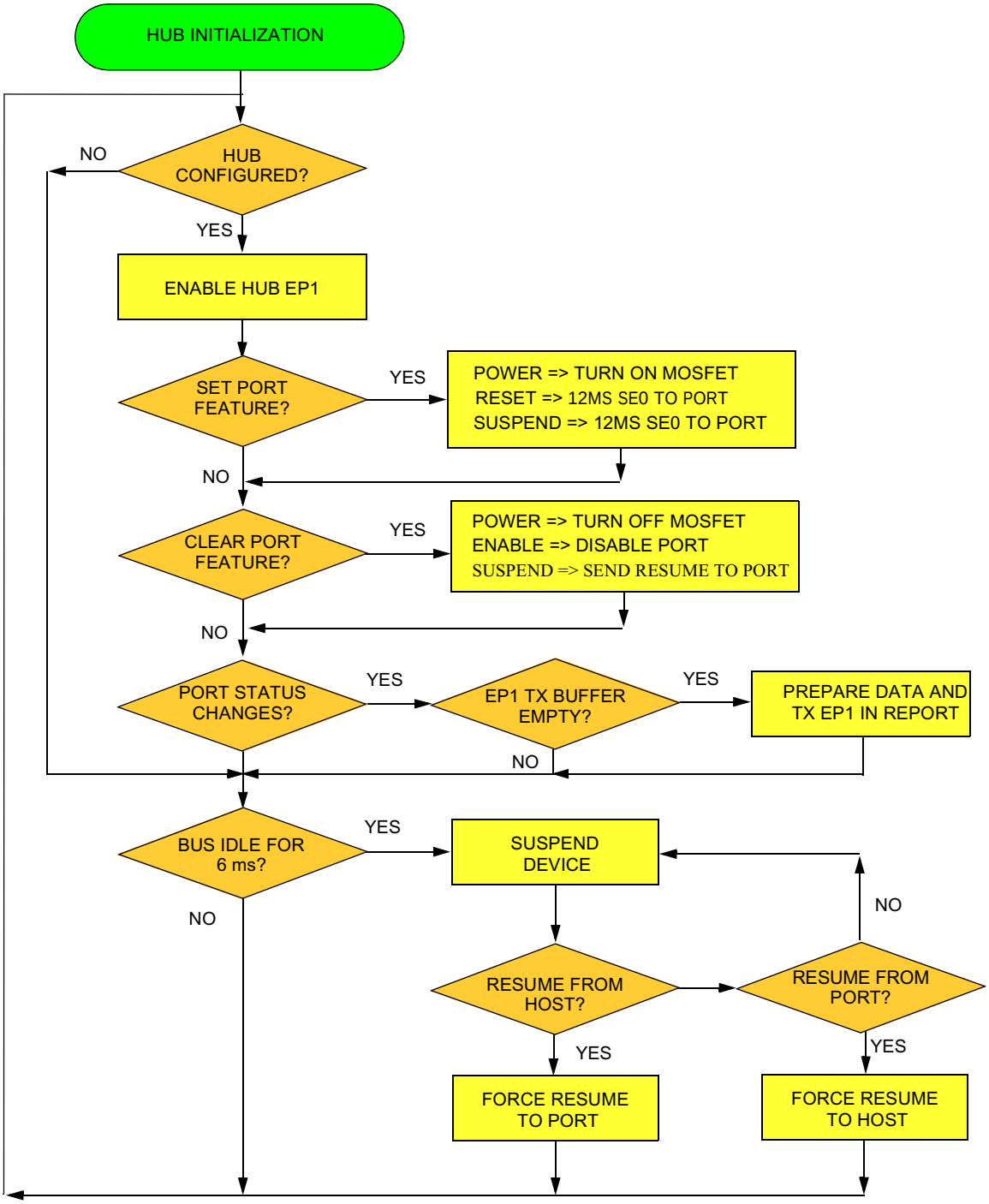

Figure 3-2. Hub Functions Routine

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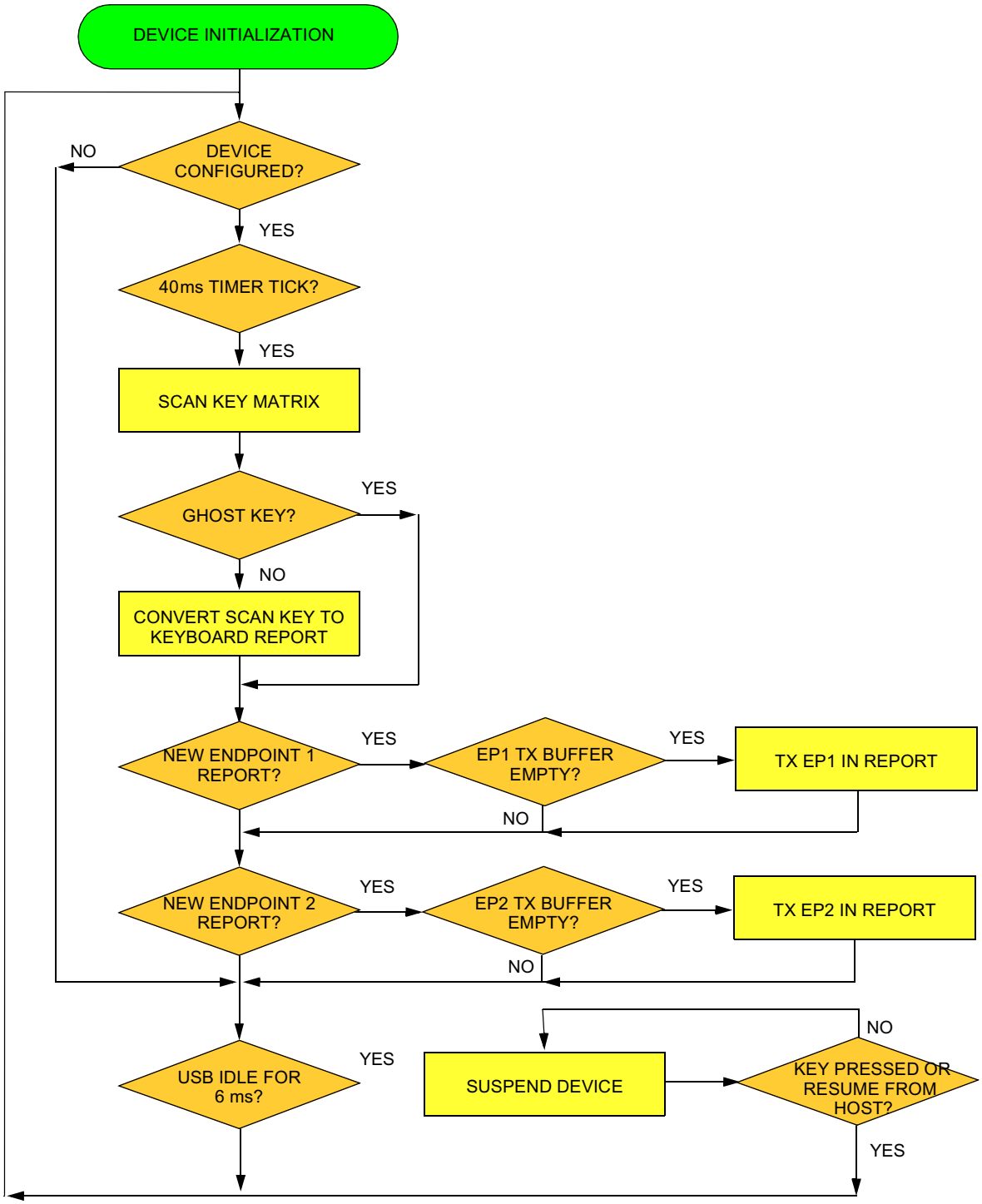

Figure 3-3. Device Functions Routine

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3.1.2 Device Functions Routine

Figure 3-3 shows the device functions routine. The routine scans the keyboard every 40ms. If there are keys pressed or released, it puts the key codes into buffer and prepares the input reports for the keys through endpoint 1 or endpoint 2. If the USB bus idles for more than 6ms, the routine puts the JB8 into STOP mode until it detects a resume signal from the host or any key pressed for remote wake-up.

3.1.3 Hub and Device Interrupt Routines

Figure 3-4 shows the hub and device interrupt routines. The USB engine automatically responds to a valid USB token with either ACK, NAK, or STALL, depending on the registers setting, and ignores it if it's invalid. The firmware has to set the registers for the USB engine to give correct response to the token in different stages. The hub interrupt is executed whenever there is SOF, EOP2, or resume signal from host is detected. The hub or the device interrupt is executed whenever there is an valid data received or data transmitted. The USB interrupt routine also makes preparation for the next USB transaction and handles any valid command or data received.

3.1.4 Control Transfer

Figure 3-5 to Figure 3-7 show the routines of handling the Control Transfers. Control transfers have two or three transaction stages: Setup, Data (optional) and Status as shown below:

- Control Write: SETUP, OUT, OUT, OUT... IN
- Control Read: SETUP, IN, IN, IN... OUT
- No Data Control: SETUP, IN

The firmware first distinguishes the kinds of control transfers and does the corresponding preparation for the next stage.

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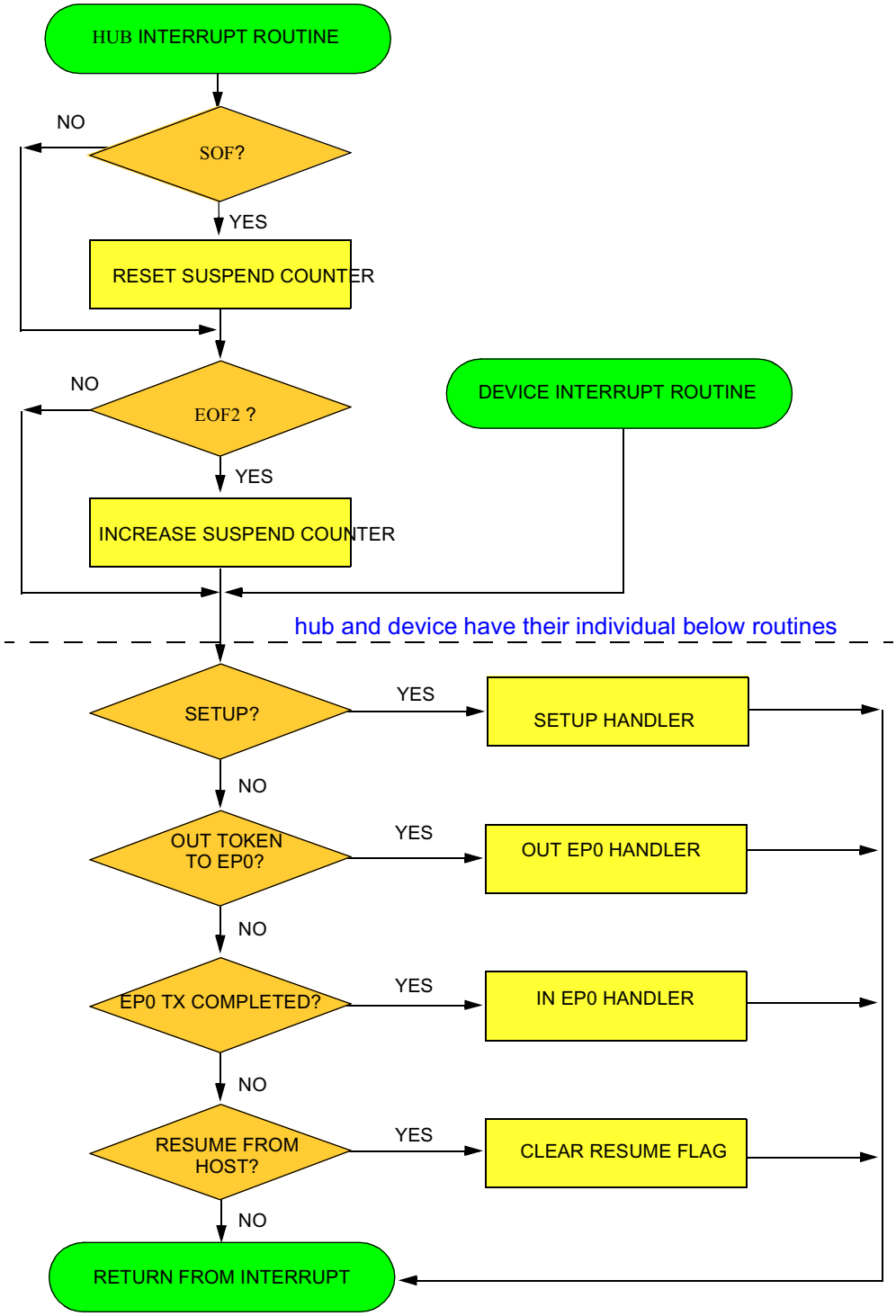

Figure 3-4. Hub and Device Interrupt Routines

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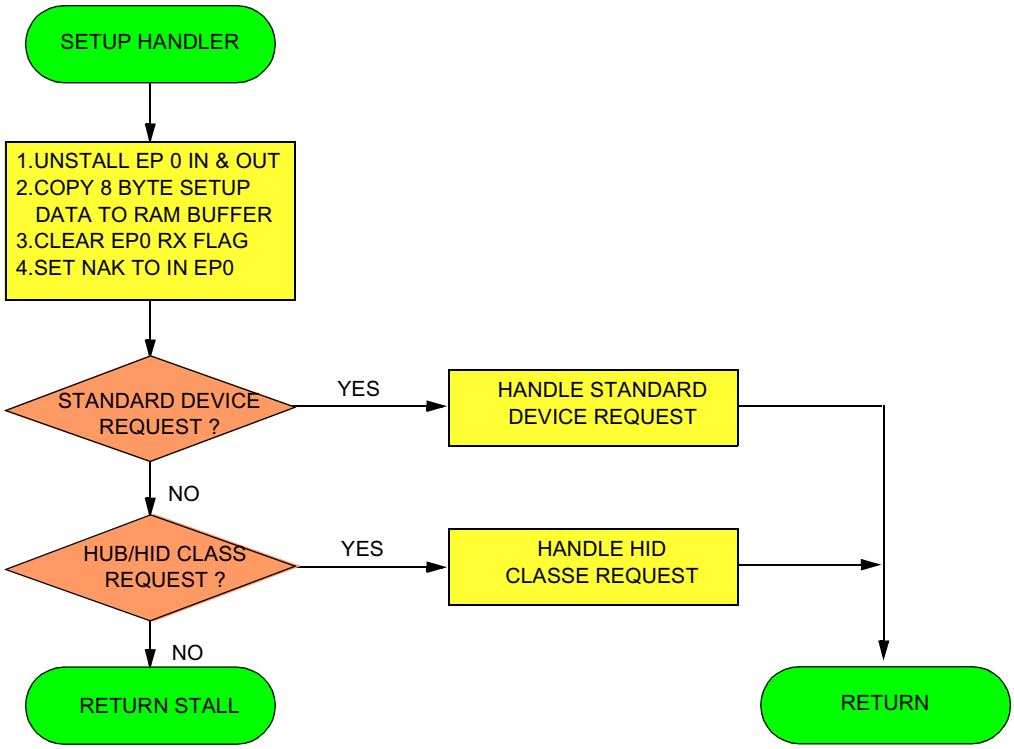

Figure 3-5. Setup Routine

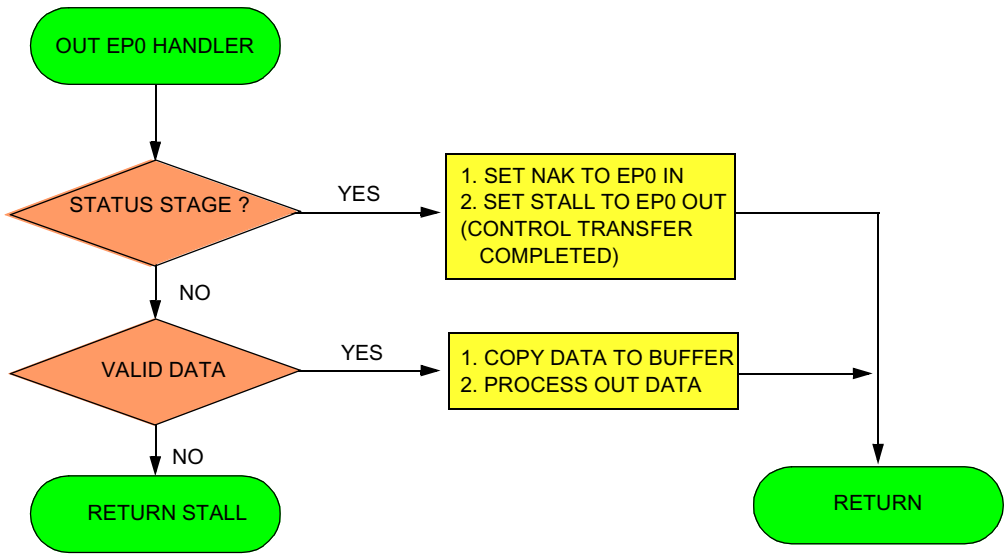

Figure 3-6. OUT Endpoint 0 Handler

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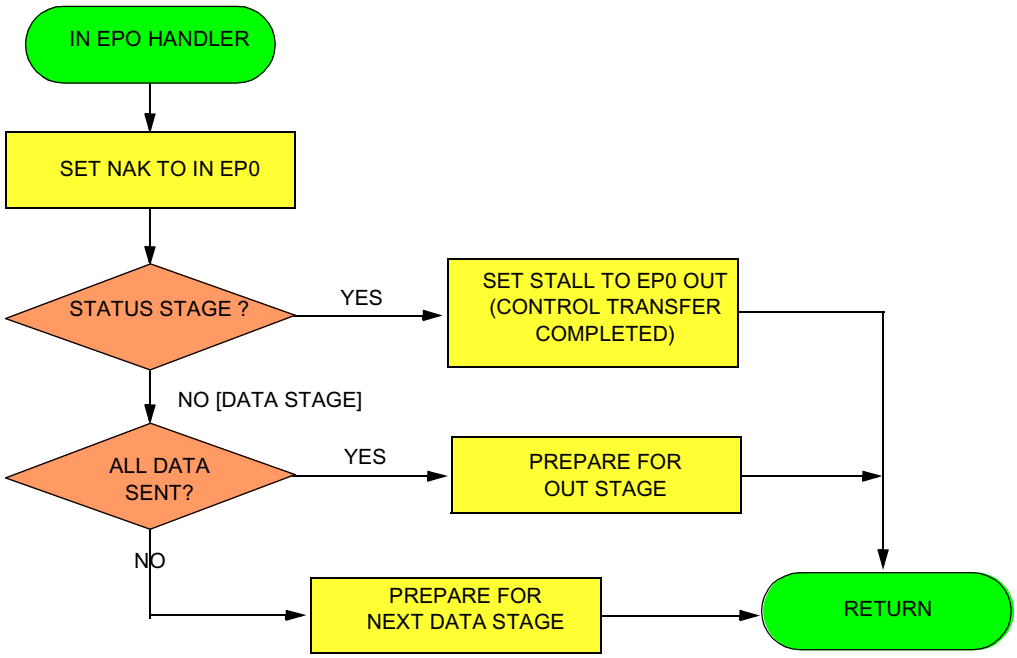

Figure 3-7. IN Endpoint 0 Handler

3.2 USB Key Codes

The key codes or usage IDs for a basic 104 keyboard are defined in the USB HID Usage Tables. In addition to the basic key codes, Microsoft has published standards for the Windows keys, Power Management keys (sleep, wake, and power), and the audio control keys as shown in Table 3-1 and Table 3-2.

Table 3-1. Consumer Page HID Controls in Windows

USAGE	USAGE NAME	DATA TYPE
$81	Power	Relative
$82	Sleep	Relative
$83	Wake	Relative

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Table 3-2. Consumer Page HID Controls in Windows ME and 2000

USAGE	USAGE NAME	USAGE TYPE	DATA TYPE
$B5	Scan Next Track	One Shot Control	Relative
$B6	Scan Previous Track	One Shot Control	Relative
$B7	Stop	One Shot Control	Relative
$CD	Play/Pause	One Shot Control	Relative
$E0	Volume	Linear Control	Relative
$E2	Mute	On/Off Control	Relative
$E3	Bass	Linear Control	Relative
$E	Treble	Linear Control	Relative
$E5	Bass Boost	On/Off Control	Relative
$E9	Volume Increment	Re-Trigger Control	Absolute
$EA	Volume Decrement	Re-Trigger Control	Absolute
$152	Bass Increment	Re-Trigger Control	Absolute
$153	Bass Decrement	Re-Trigger Control	Absolute
$154	Treble Increment	Re-Trigger Control	Absolute
$155	Treble Decrement	Re-Trigger Control	Absolute
$18A	AL Email Reader	Selector	Relative
$221	Bass Increment	Selector	Relative
$223	Bass Increment	Selector	Relative
$224	Bass Increment	Selector	Relative
$225	Bass Increment	Selector	Relative
$226	Bass Increment	Selector	Relative
$227	Bass Increment	Selector	Relative
$183	AL Consumer Control[1] Configuration	Selector	Relative
$192	AL Calculator[1]	Selector	Relative
$194	AL Local Browser[1]	Selector	Relative

1. Currently supported in Windows ME only.

3.2.1 USB Keyboard Report

The keyboard implements two HID interfaces on endpoint 1 and 2 in a USB composite-device fashion. HID interface 0 (endpoint 1) implements a standard HID keyboard with identical report and boot protocols. HID interface 1 (endpoint 2) implements multimedia and power management keys. This implementation ensures the keyboard work in BIOS setup and in DOS mode.

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Interface 0 will issue 8-byte input reports that are identical to the standard keyboard boot protocol report (see Table 3-3) as documented in the Device Class Definition for Human Interface Device (HID) version 1.1. This interface also allows the host system to turn on and off the respective LED state indicators, as specified by the 1-byte output report (see Table 3-4).

Table 3-3. Interface 0 Input Report

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Right GUI	Right ALT	Right Shift	Right Control	Left GUI	Left ALT	Left Shift	Left Control
1	Reserved							
2	Keyboard Usage ID (Key Code)							
3	Keyboard Usage ID (Key Code)							
4	Keyboard Usage ID (Key Code)							
5	Keyboard Usage ID (Key Code)							
6	Keyboard Usage ID (Key Code)							
7	Keyboard Usage ID (Key Code)							

Table 3-4. Interface 0 Output Report

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0				Kana	Compose	Scroll Lock	Caps Lock	Num Lock

Interface 1 issues power management key or multimedia key input reports, which are distinguished by a unique Report ID. The power management key uses Report ID number 1 and the multimedia key uses Report ID number 2 (see Table 3-5 and Table 3-6).

Table 3-5. Interface 1 Power Key Input Report

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Report ID = 1							
1						Power	Wake	Sleep

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Table 3-6. Interface 1 Multimedia Key Input Report

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Report ID = 2							
1	M7	M6	M5	M4	M3	M2	M1	M0
2	M15	M14	M13	M12	M11	M10	M9	M8
3	M23	M22	M21	M20	M19	M18	M17	M16
4	Reserved for M24 - M31							

Table 3-7 shows some input report examples. Report ID is not used in interface 0. The first byte is the modifier byte and is set on bit basis. Whenever a modifier key is pressed, the corresponding bit is set to one. For example, if the Left Control and the character “A” keys are pressed, the first byte of the report equals $01, the second byte is reserved, the third byte equals $04, and the forth to the eight bytes equal $00.

Power Management keys are reported through interface 1 with report ID 1. For example, if the Wake key is pressed, the first byte of report ID equals $01, and the second byte equals $02 since Wake key is defined as the bit 2 of the second byte

Hot keys are reported through interface 1 with reported ID 2. For example, if hot key 0 and hot key 17 are pressed, the first byte of report ID equals $02, the second byte equals $01 since hot key 0 is pressed, the third byte equals $00 as hot keys 8 to 16 are not pressed, and the forth byte equals $02 since hot key 17 is pressed.

Table 3-7. Input Report Examples

Keys Pressed	Endpoint	In Report Data
Left Control, ’A’	1	$01,$00,$04,$00,$00,$00,$00,$00
Left Control, Right Alt, ’A’, ’B’	1	$41,$00,$04,$05,$00,$00,$00,$00
Wake	2	$01,$02
Hot Key 0 & Hot Key 17	2	$02,$01,$00,$02

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3.3 Firmware Files

Firmware is compiled under CASM08Z.EXE version 3.16 from P&E Microcomputer Systems, Inc.

Table 3-8 summarizes the functions of each firmware files:

Table 3-8. Input Report Examples

Files	Functions
KH12-KBD.ASM	Define constants and variables Hub functions Device functions Timer interrupt
KBD-SCAN.ASM	USB key scan USB key handler
KEY-MAP.ASM	USB key matrix
HUB-CMD.ASM	USB standard device requests handler USB hub class requests handler
KBD-CMD.ASM	USB standard device requests handler USB HID class requests handler
HUB-INT.ASM	USB hub interrupt USB hub control transfer handler
DEV-INT.ASM	USB device interrupt USB device control transfer handler
MACRO8.ASM	HC08 Macro
USB-HUB.H	Device, configure, interface, endpoint, string and hub class descriptors for hub
USB-KBD.H	Device, configure, interface, HID, endpoint, string and report descriptors for keyboard
KH12-EQS.H	KH12 registers and memory definitions

Figure 3-8

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Section 4. Testing and Customization

4.1 Testing

The solution was tested under different Windows operating systems on several brands of PCs.

- USB compliance test using Command Verifier version 1.1
- Compatibility tests under Windows 98SE, 2000 and XP.
- Compatibility tests under AMD 750, Intel 810 and 845 chip set Desktops, and IBM Thinkpad 570, 600E, 600X and T23.

4.2 Customization

4.2.1 Hardware

- Left unused row and column lines unconnected as they are pulled high by internal resistors.

4.2.2 Firmware

- For unused downstream ports; connect D+ & D- lines through 100K resistors to GND, OVR line to Vdd, & PWRSW line left unconnected
- Modify the key matrix tables in “KEY-MAP.ASM” according to customized key matrix layout
- Change vendor ID, product ID and product revision number in the device descriptor table in “USB-HUB.H” and “USB-KEY.H”
- Change vendor name and product name in the string descriptor table in “USB-HUB.H” and “USB-KEY.H”

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- Change the report descriptor in “USB-KEY.H” if further Information is necessary

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Section 5. Glossary

A — See “accumulator (A).”

accumulator (A) — An 8-bit general-purpose register in the CPU08. The CPU08 uses the accumulator to hold operands and results of arithmetic and logic operations.

acquisition mode — A mode of PLL operation during startup before the PLL locks on a frequency. Also see “tracking mode.”

address bus — The set of wires that the CPU or DMA uses to read and write memory locations.

addressing mode — The way that the CPU determines the operand address for an instruction. The M68HC08 CPU has 16 addressing modes.

ALU — See “arithmetic logic unit (ALU).”

arithmetic logic unit (ALU) — The portion of the CPU that contains the logic circuitry to perform arithmetic, logic, and manipulation operations on operands.

asynchronous — Refers to logic circuits and operations that are not synchronized by a common reference signal.

baud rate — The total number of bits transmitted per unit of time.

BCD — See “binary-coded decimal (BCD).”

binary — Relating to the base 2 number system.

binary number system — The base 2 number system, having two digits, 0 and 1. Binary arithmetic is convenient in digital circuit design because digital circuits have two permissible voltage levels, low and high. The binary digits 0 and 1 can be interpreted to correspond to the two digital voltage levels.

binary-coded decimal (BCD) — A notation that uses 4-bit binary numbers to represent the 10 decimal digits and that retains the same positional structure of a decimal number. For example, 234 (decimal) = 0010 0011 0100 (BCD)

bit — A binary digit. A bit has a value of either logic 0 or logic 1.

branch instruction — An instruction that causes the CPU to continue processing at a memory location other than the next sequential address.

break module — A module in the M68HC08 Family. The break module allows software to halt program execution at a programmable point in order to enter a background routine.

breakpoint — A number written into the break address registers of the break module. When a number appears on the internal address bus that is the same as the number in the break address registers, the CPU executes the software interrupt instruction (SWI).

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break interrupt — A software interrupt caused by the appearance on the internal address bus of the same value that is written in the break address registers.

bus — A set of wires that transfers logic signals.

bus clock — The bus clock is derived from the CGMOUT output from the CGM. The bus clock frequency, f_{op}, is equal to the frequency of the oscillator output, CGMXCLK, divided by four.

byte — A set of eight bits.

C — The carry/borrow bit in the condition code register. The CPU08 sets the carry/borrow bit when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some logical operations and data manipulation instructions also clear or set the carry/borrow bit (as in bit test and branch instructions and shifts and rotates).

CCR — See “condition code register.”

central processor unit (CPU) — The primary functioning unit of any computer system. The CPU controls the execution of instructions.

CGM — See “clock generator module (CGM).”

clear — To change a bit from logic 1 to logic 0; the opposite of set.

clock — A square wave signal used to synchronize events in a computer.

clock generator module (CGM) — A module in the M68HC08 Family. The CGM generates a base clock signal from which the system clocks are derived. The CGM may include a crystal oscillator circuit and or phase-locked loop (PLL) circuit.

comparator — A device that compares the magnitude of two inputs. A digital comparator defines the equality or relative differences between two binary numbers.

computer operating properly module (COP) — A counter module in the M68HC08 Family that resets the MCU if allowed to overflow.

condition code register (CCR) — An 8-bit register in the CPU08 that contains the interrupt mask bit and five bits that indicate the results of the instruction just executed.

control bit — One bit of a register manipulated by software to control the operation of the module.

control unit — One of two major units of the CPU. The control unit contains logic functions that synchronize the machine and direct various operations. The control unit decodes instructions and generates the internal control signals that perform the requested operations. The outputs of the control unit drive the execution unit, which contains the arithmetic logic unit (ALU), CPU registers, and bus interface.

COP — See “computer operating properly module (COP).”

counter clock — The input clock to the TIM counter. This clock is the output of the TIM prescaler.

CPU — See “central processor unit (CPU).”

CPU08 — The central processor unit of the M68HC08 Family.

CPU clock — The CPU clock is derived from the CGMOUT output from the CGM. The CPU clock frequency is equal to the frequency of the oscillator output, CGMXCLK, divided by four.

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CPU cycles — A CPU cycle is one period of the internal bus clock, normally derived by dividing a crystal oscillator source by two or more so the high and low times will be equal. The length of time required to execute an instruction is measured in CPU clock cycles.

CPU registers — Memory locations that are wired directly into the CPU logic instead of being part of the addressable memory map. The CPU always has direct access to the information in these registers. The CPU registers in an M68HC08 are:

- A (8-bit accumulator)
- H:X (16-bit index register)
- SP (16-bit stack pointer)
- PC (16-bit program counter)
- CCR (condition code register containing the V, H, I, N, Z, and C bits)

CSIC — customer-specified integrated circuit

cycle time — The period of the operating frequency: $t_{CYC} = 1/f_{OP}$.

decimal number system — Base 10 numbering system that uses the digits zero through nine.

direct memory access module (DMA) — A M68HC08 Family module that can perform data transfers between any two CPU-addressable locations without CPU intervention. For transmitting or receiving blocks of data to or from peripherals, DMA transfers are faster and more code-efficient than CPU interrupts.

DMA — See “direct memory access module (DMA).”

DMA service request — A signal from a peripheral to the DMA module that enables the DMA module to transfer data.

duty cycle — A ratio of the amount of time the signal is on versus the time it is off. Duty cycle is usually represented by a percentage.

EEPROM — Electrically erasable, programmable, read-only memory. A nonvolatile type of memory that can be electrically reprogrammed.

EPROM — Erasable, programmable, read-only memory. A nonvolatile type of memory that can be erased by exposure to an ultraviolet light source and then reprogrammed.

exception — An event such as an interrupt or a reset that stops the sequential execution of the instructions in the main program.

external interrupt module (IRQ) — A module in the M68HC08 Family with both dedicated external interrupt pins and port pins that can be enabled as interrupt pins.

fetch — To copy data from a memory location into the accumulator.

firmware — Instructions and data programmed into nonvolatile memory.

free-running counter — A device that counts from zero to a predetermined number, then rolls over to zero and begins counting again.

full-duplex transmission — Communication on a channel in which data can be sent and received simultaneously.

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H — The upper byte of the 16-bit index register (H:X) in the CPU08.

H — The half-carry bit in the condition code register of the CPU08. This bit indicates a carry from the low-order four bits of the accumulator value to the high-order four bits. The half-carry bit is required for binary-coded decimal arithmetic operations. The decimal adjust accumulator (DAA) instruction uses the state of the H and C bits to determine the appropriate correction factor.

hexadecimal — Base 16 numbering system that uses the digits 0 through 9 and the letters A through F.

high byte — The most significant eight bits of a word.

illegal address — An address not within the memory map

illegal opcode — A nonexistent opcode.

I — The interrupt mask bit in the condition code register of the CPU08. When I is set, all interrupts are disabled.

index register (H:X) — A 16-bit register in the CPU08. The upper byte of H:X is called H. The lower byte is called X. In the indexed addressing modes, the CPU uses the contents of H:X to determine the effective address of the operand. H:X can also serve as a temporary data storage location.

input/output (I/O) — Input/output interfaces between a computer system and the external world. A CPU reads an input to sense the level of an external signal and writes to an output to change the level on an external signal.

instructions — Operations that a CPU can perform. Instructions are expressed by programmers as assembly language mnemonics. A CPU interprets an opcode and its associated operand(s) and instruction.

interrupt — A temporary break in the sequential execution of a program to respond to signals from peripheral devices by executing a subroutine.

interrupt request — A signal from a peripheral to the CPU intended to cause the CPU to execute a subroutine.

I/O — See “input/output (I/0).”

IRQ — See “external interrupt module (IRQ).”

jitter — Short-term signal instability.

latch — A circuit that retains the voltage level (logic 1 or logic 0) written to it for as long as power is applied to the circuit.

latency — The time lag between instruction completion and data movement.

least significant bit (LSB) — The rightmost digit of a binary number.

logic 1 — A voltage level approximately equal to the input power voltage (V_{DD}).

logic 0 — A voltage level approximately equal to the ground voltage (V_{SS}).

low byte — The least significant eight bits of a word.

low voltage inhibit module (LVI) — A module that monitors power supply voltage.

LVI — See “low voltage inhibit module (LVI).”

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M68HC08 — A Motorola family of 8-bit MCUs.

mark/space — The logic 1/logic 0 convention used in formatting data in serial communication.

mask — 1. A logic circuit that forces a bit or group of bits to a desired state. 2. A photomask used in integrated circuit fabrication to transfer an image onto silicon.

mask option — A optional microcontroller feature that the customer chooses to enable or disable.

mask option register (MOR) — An EPROM location containing bits that enable or disable certain MCU features.

MCU — Microcontroller unit. See “microcontroller.”

memory location — Each M68HC08 memory location holds one byte of data and has a unique address. To store information in a memory location, the CPU places the address of the location on the address bus, the data information on the data bus, and asserts the write signal. To read information from a memory location, the CPU places the address of the location on the address bus and asserts the read signal. In response to the read signal, the selected memory location places its data onto the data bus.

memory map — A pictorial representation of all memory locations in a computer system.

microcontroller — Microcontroller unit (MCU). A complete computer system, including a CPU, memory, a clock oscillator, and input/output (I/O) on a single integrated circuit.

modulo counter — A counter that can be programmed to count to any number from zero to its maximum possible modulus.

monitor ROM — A section of ROM that can execute commands from a host computer for testing purposes.

MOR — See “mask option register (MOR).”

most significant bit (MSB) — The leftmost digit of a binary number.

multiplexer — A device that can select one of a number of inputs and pass the logic level of that input on to the output.

N — The negative bit in the condition code register of the CPU08. The CPU sets the negative bit when an arithmetic operation, logical operation, or data manipulation produces a negative result.

nibble — A set of four bits (half of a byte).

object code — The output from an assembler or compiler that is itself executable machine code, or is suitable for processing to produce executable machine code.

opcode — A binary code that instructs the CPU to perform an operation.

open-drain — An output that has no pullup transistor. An external pullup device can be connected to the power supply to provide the logic 1 output voltage.

operand — Data on which an operation is performed. Usually a statement consists of an operator and an operand. For example, the operator may be an add instruction, and the operand may be the quantity to be added.

oscillator — A circuit that produces a constant frequency square wave that is used by the computer as a timing and sequencing reference.

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Glossary

OTPROM — One-time programmable read-only memory. A nonvolatile type of memory that cannot be reprogrammed.

overflow — A quantity that is too large to be contained in one byte or one word.

page zero — The first 256 bytes of memory (addresses $0000–$00FF).

parity — An error-checking scheme that counts the number of logic 1s in each byte transmitted. In a system that uses odd parity, every byte is expected to have an odd number of logic 1s. In an even parity system, every byte should have an even number of logic 1s. In the transmitter, a parity generator appends an extra bit to each byte to make the number of logic 1s odd for odd parity or even for even parity. A parity checker in the receiver counts the number of logic 1s in each byte. The parity checker generates an error signal if it finds a byte with an incorrect number of logic 1s.

PC — See “program counter (PC).”

peripheral — A circuit not under direct CPU control.

phase-locked loop (PLL) — A oscillator circuit in which the frequency of the oscillator is synchronized to a reference signal.

PLL — See “phase-locked loop (PLL).”

pointer — Pointer register. An index register is sometimes called a pointer register because its contents are used in the calculation of the address of an operand, and therefore points to the operand.

polarity — The two opposite logic levels, logic 1 and logic 0, which correspond to two different voltage levels, V_{DD} and V_{SS}.

polling — Periodically reading a status bit to monitor the condition of a peripheral device.

port — A set of wires for communicating with off-chip devices.

prescaler — A circuit that generates an output signal related to the input signal by a fractional scale factor such as 1/2, 1/8, 1/10 etc.

program — A set of computer instructions that cause a computer to perform a desired operation or operations.

program counter (PC) — A 16-bit register in the CPU08. The PC register holds the address of the next instruction or operand that the CPU will use.

pull — An instruction that copies into the accumulator the contents of a stack RAM location. The stack RAM address is in the stack pointer.

pullup — A transistor in the output of a logic gate that connects the output to the logic 1 voltage of the power supply.

pulse-width — The amount of time a signal is on as opposed to being in its off state.

pulse-width modulation (PWM) — Controlled variation (modulation) of the pulse width of a signal with a constant frequency.

push — An instruction that copies the contents of the accumulator to the stack RAM. The stack RAM address is in the stack pointer.

PWM period — The time required for one complete cycle of a PWM waveform.

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RAM — Random access memory. All RAM locations can be read or written by the CPU. The contents of a RAM memory location remain valid until the CPU writes a different value or until power is turned off.

RC circuit — A circuit consisting of capacitors and resistors having a defined time constant.

read — To copy the contents of a memory location to the accumulator.

register — A circuit that stores a group of bits.

reserved memory location — A memory location that is used only in special factory test modes. Writing to a reserved location has no effect. Reading a reserved location returns an unpredictable value.

reset — To force a device to a known condition.

ROM — Read-only memory. A type of memory that can be read but cannot be changed (written). The contents of ROM must be specified before manufacturing the MCU.

SCI — See “serial communication interface module (SCI).”

serial — Pertaining to sequential transmission over a single line.

serial communications interface module (SCI) — A module in the M68HC08 Family that supports asynchronous communication.

serial peripheral interface module (SPI) — A module in the M68HC08 Family that supports synchronous communication.

set — To change a bit from logic 0 to logic 1; opposite of clear.

shift register — A chain of circuits that can retain the logic levels (logic 1 or logic 0) written to them and that can shift the logic levels to the right or left through adjacent circuits in the chain.

signed — A binary number notation that accommodates both positive and negative numbers. The most significant bit is used to indicate whether the number is positive or negative, normally logic 0 for positive and logic 1 for negative. The other seven bits indicate the magnitude of the number.

software — Instructions and data that control the operation of a microcontroller.

software interrupt (SWI) — An instruction that causes an interrupt and its associated vector fetch.

SPI — See “serial peripheral interface module (SPI).”

stack — A portion of RAM reserved for storage of CPU register contents and subroutine return addresses.

stack pointer (SP) — A 16-bit register in the CPU08 containing the address of the next available storage location on the stack.

start bit — A bit that signals the beginning of an asynchronous serial transmission.

status bit — A register bit that indicates the condition of a device.

stop bit — A bit that signals the end of an asynchronous serial transmission.

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subroutine — A sequence of instructions to be used more than once in the course of a program. The last instruction in a subroutine is a return from subroutine (RTS) instruction. At each place in the main program where the subroutine instructions are needed, a jump or branch to subroutine (JSR or BSR) instruction is used to call the subroutine. The CPU leaves the flow of the main program to execute the instructions in the subroutine. When the RTS instruction is executed, the CPU returns to the main program where it left off.

synchronous — Refers to logic circuits and operations that are synchronized by a common reference signal.

TIM — See “timer interface module (TIM).”

timer interface module (TIM) — A module used to relate events in a system to a point in time.

timer — A module used to relate events in a system to a point in time.

toggle — To change the state of an output from a logic 0 to a logic 1 or from a logic 1 to a logic 0.

tracking mode — Mode of low-jitter PLL operation during which the PLL is locked on a frequency. Also see “acquisition mode.”

two’s complement — A means of performing binary subtraction using addition techniques. The most significant bit of a two’s complement number indicates the sign of the number (1 indicates negative). The two’s complement negative of a number is obtained by inverting each bit in the number and then adding 1 to the result.

unbuffered — Utilizes only one register for data; new data overwrites current data.

unimplemented memory location — A memory location that is not used. Writing to an unimplemented location has no effect. Reading an unimplemented location returns an unpredictable value. Executing an opcode at an unimplemented location causes an illegal address reset.

V —The overflow bit in the condition code register of the CPU08. The CPU08 sets the V bit when a two's complement overflow occurs. The signed branch instructions BGT, BGE, BLE, and BLT use the overflow bit.

variable — A value that changes during the course of program execution.

VCO — See “voltage-controlled oscillator.”

vector — A memory location that contains the address of the beginning of a subroutine written to service an interrupt or reset.

voltage-controlled oscillator (VCO) — A circuit that produces an oscillating output signal of a frequency that is controlled by a dc voltage applied to a control input.

waveform — A graphical representation in which the amplitude of a wave is plotted against time.

wired-OR — Connection of circuit outputs so that if any output is high, the connection point is high.

word — A set of two bytes (16 bits).

write — The transfer of a byte of data from the CPU to a memory location.

X — The lower byte of the index register (H:X) in the CPU08.

Z — The zero bit in the condition code register of the CPU08. The CPU08 sets the zero bit when an arithmetic operation, logical operation, or data manipulation produces a result of $00.

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