Single Phase On-Line
UPS Using MC9S12E128

Designer Reference Manual

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Single Phase On-Line UPS Using MC9S12E128
Designer Reference Manual

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Chapter 1
Introduction

1.1 Application Outline
This reference design describes the design of a single phase on-line uninterruptable power supply (UPS). UPSs are used to protect sensitive electrical equipment such as computers, workstations, servers, and other power-sensitive systems.

This reference design focuses on the digital control of key parts of the UPS system. It includes control of a power factor correction (PFC), a dc/dc step-up converter, a battery charger, and an output inverter. The dc/dc converter and the output inverter are fully digitally controlled. The PFC and the battery charger are implemented by a mixed approach, where an MCU controls the signals for PFC current and battery current demands. The digital control is based on Freescale Semiconductor's MC9S12E128 microcontroller, which is intended for UPS applications.

The reference design incorporates both hardware and software parts of the system including hardware schematics.

1.2 UPS Topologies and Features
UPSs are divided into several categories according to their features, which come from the hardware topologies used. The three basic categories are:

- Passive standby UPS
- Line-interactive UPS
- On-line UPS

The category of the UPS defines the basic behaviors of the UPS, mainly the quality of the output voltage and the capability to eliminate different failures on the power line (power sags, surge, under voltage, over voltage, noise, frequency variation, and so on).

NOTE
Although specific tools, suppliers, and methods are mentioned in this document, Freescale Semiconductor does not recommend or endorse any particular methodology, tool, or vendor.
1.2.1 Passive Standby UPS Topology

The common topology of the passive standby UPS is depicted in Figure 1-1.

![Figure 1-1. Passive Standby UPS Topology](image)

During normal operation, while the mains line (the power cord for the ac line) is available, the load is directly connected to the mains. The battery is charged by the charger, if necessary. If a power failure occurs, the switch switches to the opposite position, and the load is powered from the batteries. An inverter converts the battery dc voltage level to an ac mains level. The inverter generates a square wave output.

The advantage of passive standby topology is its low cost and high efficiency. The disadvantage is limited protection against power failures. Because the load is connected to the mains line through the filter only, the load is saved against short sags and surges.
1.2.2 Line-Interactive UPS Topology

The improved topology, called line-interactive, is showed in Figure 1-2. The functionality of the line-interactive UPS is similar to passive standby topology. During normal operation, the load is connected directly to the mains line (the power cord to the ac line). Besides the input filter, there is a transformer with taps connected between the mains line and the load. The transformer usually has three taps. It ensures that the output voltage can be increased or decreased relative to the mains line by typically 10 to 15%.

The features of the line-interactive topology are similar to passive standby UPSs. The cost is still quite low and efficiency is high. The protection against power failures is improved by the possibility of keeping the output voltage within limits during under voltage or over voltage using the tap transformer.
1.2.3 On-Line UPS Topology

Another topology, called on-line, is shown in Figure 1-3. This topology is also called double conversion. This name arises from the operating principle of an on-line UPS. When the UPS works in normal operation mode, while the mains line (or the power cord for the ac line) is available, the input voltage is rectified to the dc bus. The power factor correction ensures a sinusoidal current in phase with the input voltage. Then the UPS behaves as a resistive load. The output inverter converts the dc bus voltage back to a pure sinusoidal voltage.

The dc/dc converter is connected to the dc bus and converts the battery voltage to the dc bus level. The converter is activated during a power failure, and delivers the energy stored in the batteries to the dc bus. The dc bus voltage is again converted to a pure sine voltage.

A battery charger is used to charge the batteries. The charger can be powered from the mains line or from the dc bus.

As can be seen, the complexity of the on-line UPS is much greater than the other two topologies described in this section. This means that the cost is higher, and the efficiency is lower due to double conversion.

However, the on-line UPS brings a much higher quality of delivered energy. The UPS generates a pure sine wave output with tight limits (typically ±2%). Besides the power failures eliminated by previous topologies, the on-line UPS avoids all the failures relating to frequency disturbance, such as frequency variation, harmonic distortion, line noise, or other shape distortions.
1.3 MC9S12E128 Advantages and Features

The MC9S12E Family is a 112-/80-pin low-cost 16-bit MCU family very suitable for UPS, SMPS, and motor control applications. All members of the MC9S12E Family contain on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), up to 256K bytes of Flash EEPROM, up to 16K bytes of RAM, three asynchronous serial communications interface modules (SCI), a serial peripheral interface (SPI), an inter-IC bus (IIC), three 4-channel 16-bit timer modules (TIM), a 6-channel 15-bit pulse-width modulator with fault protection module (PMF), a 6-channel 8-bit pulse width modulator (PWM), a 16-channel 10-bit analog-to-digital converter (ATD), and two 1-channel 8-bit digital-to-analog converters (DAC).

The basic features of the key peripherals dedicated for UPS applications are listed below:

- Two 1-channel digital-to-analog converters (DAC) with 8-bit resolution
- Analog-to-digital converter (ATD)
  - 16-channel module with 10-bit resolution
  - External conversion trigger capability
- Three 4-channel timers (TIM)
  - Programmable input capture or output compare channels
  - Simple PWM mode
  - Counter modulo reset
  - External event counting
  - Gated time accumulation
- 6 PWM channels (PWM)
  - Programmable period and duty cycle
  - 8-bit 6-channel or 16-bit 3-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
- 6-channel pulse width modulator with fault protection (PMF)
  - Three independent 15-bit counters with synchronous mode
  - Complementary channel operation
  - Edge and center aligned PWM signals
  - Programmable dead time insertion
  - Integral reload rates from 1 to 16
  - Four fault protection shut down input pins
  - Three current sense input pins

The MC9S12E Family is powerful enough to control on-line and line-interactive UPS topologies. The passive standby topology can be controlled by a simpler MCU (from the HC08 Family).

Digital control has many advantages over separate analog control. Digital control is more flexible and allows easier tuning and changing of the UPS parameters. The intercommunication and interaction between all modules can implemented very efficiently because all modules are controlled by a single MCU.

The UPS control area is very wide. Each topology can be implemented by different circuits. The circuits may differ by different control requirements. This reference design shows one of the ways to implement digital control of an on-line UPS. The design mainly focuses on low cost. A low-cost 16-bit MCU is used with simple analog circuits. Using a mixed approach to battery charging can also be cheaper than full digital control, depending on chosen circuit topology.
Chapter 2
System Description

2.1 System Concept

The system concept of the UPS is shown in Figure 2-1. Input consists of a rectifier (D1, D5) and a power factor correction (L1, D2, Q2). The power factor correction is controlled by a mixed approach. The dc-bus voltage control loop of PFC is controlled by the MCU. The output of the voltage controller defines the amplitude of the input current. Based on the required amplitude, the MCU generates a current reference signal. The current reference signal inputs to an external logic, which performs current controller working in hysteresis mode.

Output is provided by an output inverter (Q1, Q3, D3, D4). The inverter converts the dc bus voltage back to a sinusoidal voltage using pulse-width modulation. The output inverter is fully controlled by the MCU and generates a pure sinusoidal waveform, free of any disturbance.

Figure 2-1. System Concept of UPS
The battery BT1 supplies a load during the backup mode. There are two 12-V batteries connected in serial. The battery voltage level 24-V is converted to ±390-V by the dc/dc step-up converter (Q4, Q5, D6-D9, L2, L3, and T1) using a push-pull topology fully controlled by the MCU.

The last part of a UPS is a battery charger. The battery charger maintains a fully charged battery. It uses a flyback topology controlled by a mixed approach. The flyback converter is controlled by a dedicated circuit and the required output voltage and current limit are set by the MCU. A dedicated circuit is used due to the lower cost compared to direct MCU control. Where a different battery charger topology is used, there is still enough MCU power to provide digital control.

The UPS consists of four PCBs. Most components are situated on the power stage (see Figure 2-2). These are all the power components (diodes, transistors, inductors, capacitors, relays, and so on) and analog sensing circuits. The power stage is connected to the mains line (power cord for the ac line) through an input line filter, realized on the next PCB (Figure 2-3).
Figure 2-4 shows the user interface PCB. It includes two buttons (ON/OFF, BYPASS), four status LEDs (on-line, on-battery, bypass, and error), and six LEDs indicating output power or remaining battery capacity. There are also two serial RS232 ports, which can be used for communication with the PC. The user interface provides an extension of the serial ports, which are implemented on the MC9S12E128 controller board.
System Description

Figure 2-5 shows a controller board for the MC9S12E128. The MC9S12E128 controller board is designed as a versatile development card for developing real-time software and hardware products to support a new generation of applications in UPS, servo and motor control, and many others.

The power of the 16-bit MC9S12E128, combined with Hall-effect/quadrature encoder interface, circuitry for automatic current profiling, over-current logic and over-voltage logic, and two isolated RS232 interfaces, makes the MC9S12E128 controller board ideal for developing and implementing many motor controlling algorithms, UPS, SMPS, as well as for learning the architecture and instruction set of the MC9S12E128 processor.

For more detailed information on the MC9S12E128 controller board, see [33].

An overall view of the assembled UPS is shown in Figure 2-6.

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2.2 System Specification

The UPS is designed to meet the features and parameters mentioned in Table 2-1.
### Table 2-1. On-Line UPS Specification

<table>
<thead>
<tr>
<th>Features</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Architecture and Concept</strong></td>
<td>Single Phase On-Line UPS using MC9S12E128</td>
</tr>
<tr>
<td></td>
<td>The UPS should be a regenerative 1-phase online type UPS with an automatic bypass feature when self check fails or is overloaded. The UPS is controlled manually from a front panel switch and from PC application software.</td>
</tr>
<tr>
<td><strong>Functional Modes</strong></td>
<td>On-line: If the input power is available, the UPS supplies a load and eliminates all possible defects on the line (online double conversion)</td>
</tr>
<tr>
<td></td>
<td>Battery: If the input power is not available, the UPS supplies a load from batteries. The backup time is given by battery capacity.</td>
</tr>
<tr>
<td></td>
<td>Bypass: The UPS directly connects its output and input, so the load is directly connected to the input line. The transition to this mode is set manually or automatically during overload or fault</td>
</tr>
<tr>
<td></td>
<td>Fault: If any fault is detected, the UPS signals fault, and if it is possible, the bypass is activated.</td>
</tr>
<tr>
<td><strong>Input</strong></td>
<td>45 to 65 Hz Operating Frequency Range</td>
</tr>
<tr>
<td></td>
<td>120 V (at 25% of load) — 280 V Operating Voltage Range for nominal mains 230 V</td>
</tr>
<tr>
<td></td>
<td>85 V to 135 V Operating Voltage Range for nominal mains 110 V</td>
</tr>
<tr>
<td></td>
<td>Power factor at input &gt; 0.95 at nominal voltage</td>
</tr>
<tr>
<td></td>
<td>Conversion efficiency &gt; 85% at nominal output power</td>
</tr>
<tr>
<td><strong>Output</strong></td>
<td>Number of output ports 6 in 2 segments</td>
</tr>
<tr>
<td></td>
<td>Output voltage selectable 110/120/200/220/230/240 V</td>
</tr>
<tr>
<td></td>
<td>Output power 725 – 750 VA at 230 V mains input voltage</td>
</tr>
<tr>
<td></td>
<td>Output power 325 – 350 VA at 110 V mains input voltage</td>
</tr>
<tr>
<td></td>
<td>Output waveform: true sine wave &lt; 5% THD</td>
</tr>
<tr>
<td></td>
<td>Output frequency 50/60 Hz +/-0.3%</td>
</tr>
<tr>
<td></td>
<td>Output load regulation +/-2% (at steady state and linear load)</td>
</tr>
<tr>
<td><strong>Battery</strong></td>
<td>Battery 2*12 V</td>
</tr>
<tr>
<td></td>
<td>Battery 7.2 Ah</td>
</tr>
<tr>
<td><strong>Communication</strong></td>
<td>2x RS232 port for communication with host PC with opto-isolation implemented on MC9S12E128 Controller Board</td>
</tr>
<tr>
<td><strong>Visual Interface</strong></td>
<td>4 LED indicators (on-line, battery, bypass, fault)</td>
</tr>
<tr>
<td></td>
<td>battery level gauge 6 levels (&lt;5/20/40/60/80/100%)</td>
</tr>
<tr>
<td></td>
<td>load level gauge 6 levels (20/40/60/80/100/&gt;100%)</td>
</tr>
<tr>
<td><strong>Control Interface</strong></td>
<td>2x buttons for user control (on/off, bypass)</td>
</tr>
<tr>
<td><strong>Audible warning</strong></td>
<td>Fault</td>
</tr>
<tr>
<td></td>
<td>Overload</td>
</tr>
<tr>
<td></td>
<td>low battery</td>
</tr>
<tr>
<td></td>
<td>lasts 5 minute</td>
</tr>
<tr>
<td><strong>Implementation</strong></td>
<td>Coding in C language according to ANSI C standard for software running on MCUs</td>
</tr>
<tr>
<td></td>
<td>Coding in assembler if needed for software running on MCUs</td>
</tr>
</tbody>
</table>
Chapter 3
UPS Control

3.1 Control Techniques
Generally, a UPS consists of several different converters. So the control techniques differ with the
converter topologies used. The presented implementation of on-line UPS includes following topologies:

- Battery charger: flyback converter (mixed control)
- PFC: boost converter (mixed control)
- dc/dc step up converter: push-pull converter (full digital control)
- Output inverter: half bridge inverter (full digital control)

3.1.1 Battery Charger Control
The battery charger uses a flyback converter topology. As described in Chapter 4 Hardware Design, the
flyback converter is controlled by a dedicated circuit in order to reduce cost. The interface between the
flyback converter and the MCU incorporates one digital output, which allows the setting of two output
voltage levels, and an analog output, which sets the current limit.

Using a dedicated circuit greatly simplifies the control algorithm. The functionality of the converter itself is
ensured by the dedicated circuit. Therefore, the battery charger software focuses on the charging
algorithm, whose software block diagram is shown in Figure 3-1.

The algorithm reads the current flowing to the batteries. The current value is compared with the maximal
and float thresholds. If the value is close to the maximal value, the battery charger state is set to bulk
charging and the output voltage level is set to the higher value (PU7 set to logic 1). If the actual current
value is between the maximal and float thresholds, the battery charger is considered to be in the
absorption state. The output voltage is still kept at a high level. As soon as the current value reaches the
float threshold, the battery charger goes to the float state, and the output voltage is set to the lower level.

The current limit is set during initialization, according to the number of batteries and their capacity.
The control algorithm is called every 50 ms.
Figure 3-1. Battery Charger Algorithm

MC9S12E128

PU7

PWM10

Output Voltage

Charging Current Limit

$\text{I}_{\text{Bat}} = \text{I}_{\text{max}}$

 Bulk mode
 Set HV level

$\text{I}_{\text{Bat}} > 0.05C$

 Absorption mode
 Set HV level

 Float mode
 Set LV level

$\text{I} > 0.05C$

 yes

 no

$\text{I} > 0.05C$

 yes

 no

Battery Voltage

AN03

Battery current

AN02
3.1.2 Power Factor Correction Control

The control algorithm of the PFC is depicted in Figure 3-2. The algorithm includes two control loops. The inner control loop maintains a sinusoidal input current. The outer loop controls the dc bus voltage. The result of the outer control loop is the desired amplitude of the input current.

The current control loop is partially performed by an external circuit. This control technique is also called “indirect PFC control”. The external circuit compares the actual input current with a sine wave reference. If the actual current crosses the lower border of sine waveform, the PFC transistor is switched on. As soon as the input current reaches the upper border, the PFC transistor is switched off. The resulting input current can be seen in Figure 3-3. Maximal switching frequency (50 kHz) corresponds to the hysteresis defined by resistors R664 and R675. (see Figure 4-20)
The software part of the current loop generates the sine wave reference. The sine wave reference is synchronized to be in phase with the input voltage. The sine wave generator is calculated every 50 µs. The sine waveform is generated directly by the D/A converter within the range of the voltage reference.

The voltage control loop is fully implemented by software. The sensed dc bus voltage is compared with the required dc bus voltage, 390 V. The difference inputs to the PI controller. The PI controller output directly defines the amplitude of the input current. The PI controller constants were experimentally tuned to get an aperiodic responds to the input step. The constants are \( P = 100 \) and \( T_I = 0.016 \) s. The voltage control loop is calculated every 1 ms.

The two hardware faults are immediately able to disable the PWM outputs in case of a dc bus over voltage. The digital output, PU8, enables/disables the external logic providing the current loop.

### 3.1.3 dc/dc Step-Up Converter Control

The dc/dc converter uses push-pull topology, which requires the PWM signals as shown in Figure 3-4. These signals can be generated by one pair of PMF outputs with the following configuration:

- even output is set to positive polarity
- odd output is set to negative polarity
- duty cycle of even output is set to \( X\% \)
- duty cycle of odd output is set to 100 - \( X\% \)

where \( X \) is a value from 0 to 50% – dead time

The required PWM patterns are shown in Figure 3-4.
The control algorithm is depicted in Figure 3-5. Both dc bus voltages pass the digital filter, and their sum is compared with the required value of the dc bus voltage. Based on the error, the PI controller sets the desired duty cycle of the switching transistors.

During mains line operation, the required value of the dc bus is set to 720 V (2 x 360 V). Because the dc bus is kept by the PFC at 780 V (2 x 390 V), the dc/dc converter is automatically switched off. In case of mains failure, the dc bus voltage will start to fall. As soon as the voltage reaches the value 720 V, the dc/dc converter is activated. At 720 V, there is still 20 V reserve in amplitude to generate a maximum output voltage of 240 V RMS. As soon as the operation from batteries is recognized, the required value of the dc bus voltage is increased back to 780 V.

The PI controller maintains the constant voltage on the dc bus independent of the load until the mains is restored or the battery is fully discharged. If the battery is discharged, the UPS output is deactivated and UPS stays in STANDBY ON BATTERY mode. After 1 minute, the UPS is switched off.

The PI controller constants were experimentally tuned in the same way as the PFC. The constants are $P = 39$ and $T_I = 0.0033$ s. The control loop is calculated every 1 ms.
### 3.1.4 Output Inverter Control

The output inverter is implemented by two IGBT transistors in half bridge topology. The inverter is fully digitally controlled and generates a pure sine wave voltage.

The sine waveform is generated using the pulse-width modulation technique. The sine reference is stored in a look-up table. The table values are periodically taken from the table, and then multiplied by the required amplitude. The resulting value gives the duty cycle of the PWM output. The pointer to the table is incremented by a value, which corresponds to the desired output frequency. All values over one period give sinusoidal modulated square wave output (see Figure 3-6). If such a signal passes through a LC filter, the pure sine wave voltage is generated on the inverter output.

![Figure 3-6. Sine Wave Modulation](image)

The control algorithm can be seen in Figure 3-7. The main control loop comprises of the PID controller and a feed forward control technique. The required value entering the PID controller is generated by a sine wave generator, optionally synchronized with input voltage. The same value is added directly to the output of the PID controller. It is called the feed forward technique, and it improves the responds of control loop. The amplitude of the sine wave reference is corrected by RMS correction, which keeps the RMS value of the output voltage independent of any load. The RMS correction uses the PI controller. The PI constants were experimentally tuned, and set to $P = 0$ and $T_I = 0.00936$.

The PID controller was tuned using simulation in MATLAB. The results of the simulation can be seen in Figure 3-8 and Figure 3-9, with $P = 0.6$, $T_I = 0$, $T_D = 0.00071$ s, and $N = 31$. The value $N$ represents the filter level of D portion EQ 3-5.

The result of the PID controller, including feed forward, is scaled relative to actual dc bus voltage. Then the exact duty cycle is set to the PMF module.
Figure 3-7. Inverter Control Algorithm

Figure 3-8. Simulated PID Controller Response on Input Step
3.1.5 PI and PID Controller

The PI controller in a continuous time domain is expressed by following equation:

\[ u(t) = K \left[ e(t) + \frac{1}{T_I} \int_0^t e(\tau) d\tau \right] \]  (EQ 3-1)

Similarly, the PID controller can be expressed as:

\[ u(t) = K \left[ e(t) + \frac{1}{T_I} \int_0^t e(\tau) d\tau + T_P \frac{d}{dt} e(t) \right] \]  (EQ 3-2)

In a Laplace domain it can be written as:

\[ u(s) = K \left[ e(s) + \frac{1}{sT_I} e(s) \right] \]  (EQ 3-3)

\[ u(s) = K \left[ e(s) + \frac{1}{sT_I} e(s) + sT_D e(s) \right] \]  (EQ 3-4)

To improve the response of the PID controller to noisy signals, the derivative portion is often replaced by a derivative portion with filter:

\[ sT_D = \frac{sT_D}{1 + sT_D N} \]  (EQ 3-5)

For implementation of algorithms on MCU the equations EQ 3-3 and EQ 3-4 have to be expressed in discrete time domain like:

\[ u(kh) = P(kh) + I(kh) + D(kh) \]  (EQ 3-6)
where

\[ P(kh) = K \cdot e(kh) \]  \hspace{1cm} (EQ 3-7)

\[ I(kh) = I(kh - h) + \frac{K_h}{T_i} e(kh) \]  \hspace{1cm} (EQ 3-8)

\[ D(kh) = \frac{T_D}{T_D + Nh} D(kh - h) - \frac{K_T D N}{T_D + Nh} e(kh - h) \]  \hspace{1cm} (EQ 3-9)

\[ e(kh) = w(kh) - m(kh) \]  \hspace{1cm} (EQ 3-10)

and

- \( e(kh) \) = Input error in step \( kh \)
- \( w(kh) \) = Desired value in step \( kh \)
- \( m(kh) \) = Measured value in step \( kh \)
- \( u(k) \) = Controller output in step \( kh \)
- \( P(kh) \) = Proportional output portion in step \( kh \)
- \( I(kh) \) = Integral output portion in step \( kh \)
- \( D(kh) \) = Derivative output portion in step \( kh \)
- \( T_I \) = Integral time constant
- \( T, h \) = Sampling time
- \( K \) = Controller gain
- \( t \) = Time
- \( s \) = Laplace variable
- \( N \) = Filter constant

### 3.1.6 Phase-Locked Loop (PLL) Algorithm

The PLL algorithm provides synchronization with the mains line. This synchronization is necessary for the PFC algorithm and can be optionally used for the inverter output.

The algorithm consists of two parts:
- Frequency lock
- Phase lock
The PLL algorithm measures a period from last two zero crossing signals. Because calculation of the phase increment to the sine wave table requires a division instruction \( \text{EQ 3-11} \), the phase over one-half period is calculated instead:

\[
\text{Phase Increment} = 32767 \frac{T}{\text{Period}}
\]  

(EQ 3-11)

where

\[
T = \text{period of sine wave algorithm (50 \, \mu s)}
\]

32767 = 180° in sine wave look up table

Period = measured period of main line voltage

If phase increment just corresponds to the measured period we should get a phase of 180°. If there is some difference, the phase increment must be adjusted (see Figure 3-10). Based on the sign of the phase difference, the phase increment is incremented or decremented by the value which is equal to the phase difference multiplied by the PLL constant.

If the phase difference falls below some limit for last 20 periods, the PLL is locked to the line frequency and a frequency locked status bit is set.

![Figure 3-10. Calculation of Phase Difference](image)

Now the PLL is running with the same frequency as the mains line, but the phase is still different. As soon as the frequency status bit is set, the actual phase is adjusted to 0° or 180° according to the previous polarity of the input voltage. The polarity of the input voltage is sensed in the middle of each period.
Chapter 4
Hardware Design

4.1 System Configuration

The single phase on-line UPS reference design is 750 VA UPS representing an on-line topology. The UPS comprises four PCBs (power stage, user interface, input filter, and controller board). The power stage together with the MC9S12E128 controller board is shown in Figure 1-2.

![Figure 4-1. System Concept of UPS](image)

The UPS reference design provides both a ready-to-use hardware and a ready-made software development platform for an on-line UPS, under 1000 VA output power, and controlled by a single 16-bit MCU.

The UPS power stage consists of several system blocks shown as:

- Battery Charger
- Auxiliary Power Supplies
- Control Board Interface
- dc/dc Step-Up Converter
- PFC + Inverter
4.2 Battery Charger

4.2.1 Operational Description

The battery charger is intended for charging the UPS batteries and supplying all UPS control circuits. The battery charger provides a three-state charging algorithm fully controlled by the MCU. Its operating parameters are listed in Table 4-1.
NOTE
The output values are set to the values recommended by the battery manufacturer. The current limits can be set to any value by SW.

4.2.2 Battery Charger Topology

The battery charger uses a flyback topology, frequently used for its simplicity for output power below 100 W. The charger consists of a flyback converter, battery voltage and current sensing, current limitation, and mains line voltage detection. The schematic of the battery charger is shown in Figure 4-3. The flyback converter uses the dedicated circuit TOP249 for control, which incorporates a MOSFET transistor and control circuit in one package. Using this dedicated circuit allows connection of the control signals to the secondary side of the flyback converter without galvanic isolation. The second advantage of the solution is that UPS power is independent of MCU control, and the UPS is able to run without batteries.
Figure 4-3. Battery Charger Schematics
4.2.3 Flyback Converter Operation

The flyback converter consists of the transformer T300, the MOSFET transistor U300 include control circuit and the feedback circuit (R303, R305, R309, R312, Q301, ISO300, and U302).

When the MOSFET transistor (U300) is switched on, the magnetic field energy is accumulated in the magnetic core of the transformer T300. During this time the output diodes (D301, D304) are reverse biased. As soon as the transistor is switched off, the accumulated magnetic field energy is released through the forward biased output diodes (D301, D304) to the output capacitors (C304, C305), and through the output filter (L300, L301, C306) to the load.

The output voltage is sensed by the divider (R303, R305, R309, R312). The voltage from the divider is compared with the internal reference of U302. The U302 creates the control signal—the current flowing through the opto coupler (ISO300)—which galvanically isolates the primary and secondary side of the flyback converter.

The control signal is connected to the control pin of the control circuit (U300). According to the control signal, the duty cycle of the MOSFET transistor (U300) is set. The MOSFET transistor is switched with a fixed frequency of 66 kHz.

The resistor R312 can be shorted by the transistor Q301. This allows setting the output voltage to either 29.4 or 27.4 V by the MCU.

4.2.4 Design of Flyback Converter

The design of flyback converter using TOP249 is described in detail in [10], [11] and [12]. The following input parameters were considered during the converter design:

<table>
<thead>
<tr>
<th>Table 4-2. Input Design Parameters of Flyback Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
</tr>
<tr>
<td>Max. output voltage</td>
</tr>
<tr>
<td>Max. output current</td>
</tr>
<tr>
<td>Switching frequency</td>
</tr>
</tbody>
</table>

The calculated parameters of the flyback transformer are specified in Table 4-3. The measured values on the manufactured sample are listed in Table 4-4. To decrease leakage inductance, the interleaved winding layout is used for the primary winding. The complete transformer winding layout is shown in Figure 4-4.
Table 4-3. Required Parameters of Flyback Transformer

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetizing inductance referred to the primary</td>
<td>328 mH + 30 – 20%</td>
</tr>
<tr>
<td>Magnetizing inductance referred to the secondary</td>
<td>31 μH + 30 – 20%</td>
</tr>
<tr>
<td>Total leakage inductance referred to the primary</td>
<td>&lt;3.5 μH</td>
</tr>
<tr>
<td>Primary dc resistance</td>
<td>&lt;0.1 Ω</td>
</tr>
<tr>
<td>Secondary dc resistance</td>
<td>&lt;0.001 Ω</td>
</tr>
<tr>
<td>Test Voltage primary-to-secondary</td>
<td>2.5kV ac</td>
</tr>
</tbody>
</table>

Table 4-4. Measured Values on the Sample

<table>
<thead>
<tr>
<th>Pin #</th>
<th>L [μH] @1kHz, 1V</th>
<th>L [μH] @100kHz, 1V</th>
<th>ESR [Ohm] @100kHz, 1V</th>
<th>DCR [Ohm]</th>
<th>L [μH] @100kHz, 1V pin # 9 and 13 shorted</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-6</td>
<td>331.2</td>
<td>330.5</td>
<td>2.142</td>
<td>0.095</td>
<td>2.88</td>
</tr>
<tr>
<td>5-7</td>
<td>5.2</td>
<td>5.22</td>
<td>0.061</td>
<td>0.018</td>
<td>-</td>
</tr>
<tr>
<td>9-13</td>
<td>29.8</td>
<td>29.74</td>
<td>0.194</td>
<td>0.0005</td>
<td>-</td>
</tr>
</tbody>
</table>
4.2.5 Voltage and Current Sensing, Current Limitation

The battery voltage is sensed by the divider (R304, R307, and R310). The divider scales the maximum measurable battery voltage of 39 V to the A/D converter range of 5 V. The battery current is sensed as the voltage drops on resistor R300. The voltage drop is amplified by U301B to get 5 V at 2.4 A.

The current limitation is provided by U301A. The U301A compares the actual battery current with the limit, which is set by the MCU. The MCU generates a PWM signal, which is filtered to the analog value.

4.2.6 Main Line Detection

The mains line detection ensures that the UPS is internally switched on (STANDBY ON LINE state) if the mains line is available. The detection circuit detects the functionality of the flyback converter, and if the mains line is detected, the power supplies are switched on. The detection circuit consists of rectified diodes D307, D308, and transistor Q302.

4.2.7 Battery Charger Algorithm

There are many algorithms (constant voltage, constant current, two stage, three stage, etc.), that can be used for charging lead acid batteries. The algorithms differ by the complexity of battery charger implementation and by influence on the battery life.

Because the battery charger is controlled by the MCU, any battery charger algorithm can be implemented. The UPS reference design uses the three stage charging algorithm (see Figure 4-5).

![Figure 4-5. 3-Stage Charging Algorithm](image-url)
As the name of the algorithm suggests, charging consists of three stages. The charging starts with the current limit 0.25 of battery capacity. The battery charger works in current mode until the battery voltage reaches the high level voltage (2.45 V/cell). This stage is called bulk charging. As soon as the battery voltage reaches the high level, the current starts to fall, and the absorption stage begins. Once the battery current falls under 0.05 of battery capacity, the battery charge voltage is set to the low level (2.28 V/cell). The last stage is called the float stage.

**NOTE**
The voltage levels and current thresholds come from the battery manufacturer. The values may also vary with the temperature if temperature measurement is implemented.

### 4.3 Auxiliary Power Supplies

Signal circuits, control circuits, digital circuits, and driving circuits are supplied by auxiliary SMPSs (Figure 4-6). Since the drive circuits have to be galvanically isolated from each other, a small isolated flyback converter (Figure 4-7) is used to generate separate voltage sources for all power semiconductor drivers.

![Figure 4-6. Auxiliary SMPSs](image-url)
Supply voltages for the microcontroller and other digital circuits (+5V_D) are generated by U202. U200 is used to stabilize +15V for the flyback converter, relays, dc/dc MOSFETs drivers, and cooling fans and it is used as a down-converter for U203 in order to lower the power loss dissipated by U203. The IC supplies 5 V for op amps, comparators, and the heatsink temperature sensor. The output voltage is further filtered and used as a reference for the signal and control circuits. In order to switch-on and switch-off all the control and signal circuits, U200 and U202 are controllable by POWER_EN and /POWER_EN signals. POWER_EN signal is driven by the microcontroller to control the switch-off process. /POWER_EN signal is grounded when the “ON” button is depressed. All the power supplies are put into an operational state, the micro starts to execute the program, and the POWER_EN signal is then put into the active state to hold the supplies operational even when the button is released.

Figure 4-7 shows the isolated flyback converter schematic that provides the inverter and PFC drivers with a power supply. MOSFET Q201 is driven by UC3843 in a classic current-mode configuration without the feedback loop. The supply is designed to deliver constant power to the output while access power is dissipated in zener diodes D202-D203, D206-D207, and D209 in case of drivers-in-standby. Respective zener diodes are used specifically to split the secondary voltage to 5-V and 15-V levels.
Figure 4-7. Isolated Flyback Converter for Drivers
4.3.1 Auxiliary SMPS Design Considerations

Auxiliary SMPS design (Figure 4-6) follows producer general considerations for LM2575 and 78L05 switched and linear regulators.

Because the isolated flyback converter is based on a standard UC384X IC, the design is focused on transformer design. The transformer is used as an energy reservoir. During the switch-on the energy is accumulated, and during the switch off the energy is delivered to the output capacitor and the load.

Respective output voltages are 2 x 20-V for HCPL315J output inverter driver - generated by L2 and L3 (+15 and –5 V are good driving margins in 800-V application), and 15-V for HCPL3150 PFC driver - generated by L4 (single supply 15 V is sufficient for 400-V application). First, the output power is defined. When driver circuits with HCPL315J and HCPL3150 drivers are considered, a value of 1.2 W is obtained. When efficiency is considered, a value of 2 W is obtained. For such power, a switching frequency 300 kHz is chosen. Let’s consider a 0.5 maximum duty. It means that during half of the switching period, all energy for the whole cycle must be accumulated in the transformer.

The average necessary input charge is given by EQ 4-1. When we consider the triangular shape of the transformer primary current, we get EQ 4-2 for the charge taken by the transformer.

\[ Q = I_{AV} \cdot T = \frac{P_{IN}}{V_{IN}} \cdot T \]  
\[ Q = \int i_{dt} = \frac{t_{ON} \cdot I_P}{2} \] 

Because the voltage is equal, the equality of these charges also provides equal energies. When we compare both equations, we get

\[ \frac{P_{IN}}{V_{IN}} \cdot T = \frac{t_{ON} \cdot I_P}{2} \]  

Rearranging EQ 4-3 we get EQ 4-4 for the peak primary current:

\[ I_{pp} = 2 \cdot \frac{P_{IN}}{V_{IN}} \cdot \frac{T}{t_{ON}} = 2 \cdot \frac{2}{15} \cdot \frac{3.3 \mu}{1.5 \mu} = 586 mA \] 

The peak secondary current for a 20-V output is calculated using EQ 4-6 (all the output power is considered), and the secondary winding inductance L2 is then given by EQ 4-7.

\[ L_1 = \frac{V_{IN}}{di}dt = \frac{15}{0.586} \cdot 1.5 \mu = 38 \mu H \] 
\[ I_{IP} = 2 \cdot \frac{P_{OUT}}{V_{OUT}} \cdot \frac{T}{t_{OFF}} = 2 \cdot \frac{1.6}{20} \cdot \frac{3.3 \mu}{1.8 \mu} = 293 mA \] 
\[ L_2 = \frac{V_{OUT}}{di}dt = \frac{20}{0.293} \cdot 1.8 \mu = 123 \mu H \]
Let’s choose a RM8 core made from N97 ferrite material, with \( A_\text{e} = 64 \text{mm}^2 \) and \( A_L = 3300 \text{nH} \). Respective winding turns are as follows:

\[
N_{1} = \frac{I_{p}}{\sqrt{A_L}} = \sqrt{\frac{38 \mu}{3300}} = 3.4 = 4t \quad \text{(EQ 4-8)}
\]

\[
N_{2} = \frac{I_{s}}{\sqrt{A_L}} = \sqrt{\frac{123 \mu}{3300}} = 6.1 = 6t \quad \text{(EQ 4-9)}
\]

Therefore, \( N_1 \) primary to \( N_2 \) secondary ratio is given as follows:

\[
p = \frac{N_{1}}{N_{2}} = \frac{4}{6} = 0.667 \quad \text{(EQ 4-10)}
\]

For supplying the PFC driver, 15-V supply voltage is necessary and the turns ratio between both secondaries is used to calculate the number of turns for the PFC driver.

\[
N_{4} = \frac{15}{20} \cdot N_{2} = \frac{15}{20} \cdot 6 = 4.5t \quad \text{(EQ 4-11)}
\]

Rounding the number up or down would cause large unbalanced secondary voltages. Secondary turns are then scaled to obtain appropriate secondary-to-secondary ratio. Afterwards, primary turns are also altered. In this case, \( N_2 = 8t \) gives exact value of \( N_4 = 6t \) as follows:

\[
N_{4} = \frac{15}{20} \cdot N_{2} = \frac{15}{20} \cdot 8 = 6t \quad \text{(EQ 4-12)}
\]

Now, the primary turns are scaled to maintain primary-to-secondary ratio:

\[
N_{1} = p \cdot N_{2} = 0.667 \cdot 8 = 5.34 = 5t \quad \text{(EQ 4-13)}
\]

To maintain a discontinued conduction mode, the switching frequency has to be also altered to the value of 200 kHz. And the maximum flux has to be checked - simulation shows flux of amplitude 160 mT.

Figure 4-8 shows the layout of the windings on the transformer bobbin.
4.4 dc/dc Step-Up Converter

4.4.1 dc/dc Converter Operational Description

A dc/dc converter is intended for dc bus supply when the UPS run from batteries. Parameter specifications are listed in Table 4-5. The converter transforms the battery voltage of 24 V to a dc bus voltage of +400 V, –400 V. Low-cost considerations led to push-pull topology as shown in Figure 4-9. The circuit consists of a push-pull inverter (Q500-Q503), power transformer T500, bridge rectifier (D500, D502, D504, D505) and filter L501, L502. The rectifier directly supplies the dc bus voltage +400,–400 V.

Table 4-5. dc/dc Converter Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage nominal</td>
<td>24 V</td>
</tr>
<tr>
<td>Input voltage minimal</td>
<td>21 V</td>
</tr>
<tr>
<td>Input voltage maximal</td>
<td>30 V</td>
</tr>
<tr>
<td>Output voltage nominal</td>
<td>+390 V -390 V</td>
</tr>
<tr>
<td>Output voltage minimal</td>
<td>+350 V -350 V</td>
</tr>
<tr>
<td>Output power nominal</td>
<td>580 W</td>
</tr>
<tr>
<td>Output current nominal</td>
<td>0.74 A</td>
</tr>
<tr>
<td>Input current nominal</td>
<td>27 A</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>50 kHz</td>
</tr>
</tbody>
</table>
Figure 4-9. dc/dc Converter Schematic
The converter performance and features are analyzed by simulation with the model shown in Figure 4-10.
Hardware Design

The inverter is supplied by a set of low-ESR capacitors, C502-C505 and C512-C513, to lower the battery bus ripple current and hence the EMI signature of the converter input. Inverter MOSFETs Q500-Q503 are driven by MC33152 drivers. MOSFETs drain voltage ringing is damped by RC cells R504-C507 and R503-C508. Because of the voltage source character of the inverter, the rectifier has to be a current type, which is why smoothing chokes L501 and L502 are used. Over voltage spikes across the rectifier diodes, due to the diodes reverse-recovery and transformer leakage, are clamped by RCD snubbers consisting of a R501- C501- D501 for the positive side, and R502 - C506 - D503 for the negative side.

4.4.2  dc/dc Converter Design Considerations

4.4.2.1  Power Transformer

The first task in power transformer design is to choose an appropriate transformer core. Based on manufacturer power-handling-capability core tables the core size is selected. Subsequently, the maximum core flux density travel $\Delta B$ must be determined from the core manufacturer data sheet, and then an approximate number of turns can be calculated. Since the number of turns is usually an integer, the number is rounded and the real flux density travel is calculated. If $\Delta B$ is below a maximum limit with respect to the switching frequency (core material dependent), winding turns and the cross-sectional areas are calculated for all respective windings.

For 580W output, an ETD44 core is selected. Now, the integral of the Faraday induction law Eq 4-14 gives the relation for the magnetic charge put into the core Eq 4-15:

$$u_i = \frac{d\psi}{dt} = N\frac{d\Phi}{dt} = N \cdot S \frac{dB}{dt}$$  \hspace{1cm} (EQ 4-14)

where

$u_i$ = induced voltage

$\psi$ = linkage flux in the core

$N$ = number of turns

$\Phi$ = flux in the core

$B$ = flux density in the core

$$\int u_i dt = N \cdot S \cdot \Delta B$$  \hspace{1cm} (EQ 4-15)

where

$\Delta B$ = flux density travel

$S$ = core cross-sectional area
Initially, the magnetic charge has to be calculated. Since the induced voltage during an active part of the converter operational cycle is constant and it equals the input voltage, the magnetic charge in the core is given by \( EQ\ 4-16 \):

\[
\int u_i dt = V_{IN} \cdot \delta \cdot T 
\]  

(EQ 4-16)

where

\[
\begin{align*}
V_{IN} & = \text{input voltage} \\
\delta & = \text{switching duty cycle} \\
T & = \text{switching period (f = 50kHz)}
\end{align*}
\]

\[
\int u_i dt = 24 \cdot 0.45 \cdot 20 \times 10^{-6} = 216 \ \mu V s 
\]  

(EQ 4-17)

Simulation results can also be used to obtain the magnetic charge. Figure 4-11 shows simulated magnetizing voltage and magnetic charge. Magnetic charge is obtained by the time integral of the magnetizing voltage. Peak-to-peak reading of the magnetic charge is 218 \( \mu \)V.

Rearranging EQ 4-15, the number of primary turns can be calculated:

\[
N_1 = \frac{\int u_i dt}{S \cdot \Delta B} = \frac{216 \times 10^{-6}}{173 \times 10^{-6} \cdot 0.4} = 3.12\ t 
\]

(EQ 4-18)
Let's choose 3 turns. However, the flux density travel $\Delta B$ has to be checked:

$$\Delta B = \int_{0}^{t} \frac{u_{i}}{S \cdot N_{1}} dt = \frac{216 \times 10^{-6}}{173 \times 10^{-6} \cdot 3} = 416 \text{ mT}$$  \hspace{1cm} (EQ 4-19)

From EPCOS Siferit N97 specification (FAL0625-W @60°C), the core power loss is 10 W, indicating a good core utilization. However, forced convection should be considered. The negative loss temperature coefficient of the N97 material is advantageous since it contributes to a temperature stability of the core (FAL0624-N).

Now, the number of turns of the secondaries can be calculated. For primary to secondary ratio and a forward type of converter, equation EQ 4-20 is valid:

$$p = \frac{V_{OUT}}{V_{IN} \cdot \eta \cdot \delta_{MAX}}$$  \hspace{1cm} (EQ 4-20)

For efficiency $\eta = 0.93$ and maximum duty $\delta_{(MAX)} = 0.98$, EQ 4-20 yields

$$p = \frac{V_{OUT}}{V_{IN} \cdot \eta \cdot \delta_{MAX}} = \frac{350}{21 \cdot 0.93 \cdot 0.97} = 18.47$$  \hspace{1cm} (EQ 4-21)

Primary to secondary ratio is rounded to 18, and the secondary winding number of turns yields

$$N_{2} = p \cdot N_{1} = 18 \cdot 3 = 54 t$$  \hspace{1cm} (EQ 4-22)

Once the winding turns are determined, the cross sectional area of a winding can be calculated. For the ETD44 core, winding current density can be selected in the range 5-10A/mm$^2$. Let $J = 8$A/mm$^2$. Primary cross-sectional area is given by EQ 4-23

$$S_{1} = \frac{I_{1}}{J} = \frac{19.1}{8} = 2.39 \text{ mm}^2$$  \hspace{1cm} (EQ 4-23)

where

$I_{1}$ = nominal primary winding current obtained by integrating the square of the simulated winding current (Figure 4-12).
Figure 4-12. Simulated Primary Winding Current

Secondary cross-sectional area is given by EQ 4-24:

\[ S_2 = \frac{I_2}{J} = \frac{0.74}{8} = 0.093 \text{ mm}^2 \quad (EQ \ 4-24) \]

where

- \( I_2 \) = nominal secondary winding current obtained by integrating the square of the simulated winding current (Figure 4-13).
Figure 4-13. Simulated Secondary Winding Current

For a 50kHz switching frequency the skin effect depth is given by EQ 4-25:

\[
\delta = \frac{0.066}{\sqrt{f}} = \frac{0.066}{\sqrt{50 \times 10^3}} = 295 \mu m
\]  

(EQ 4-25)

In this case the best solution for the primary is the use of a copper foil. An ETD44 bobbin has a width of 30 mm. Because of the necessary creepage, the foil width is set to 25 mm. Based on the result of EQ 4-23, the foil thickness yields 100 µm and has excellent skin performance when compared with skin depth at the current switching frequency.

From the result of EQ 4-24, the secondary winding wire diameter yields 0.338 mm. The nearest wire diameter in production is 0.315mm. A wire with a larger diameter is not helpful any more because of the increased ac resistance due to the skin effect.

The primary winding of the push-pull converter transformer uses a center-tapped windings as well as the secondary windings. As the power transformer is a part of the push-pull converter, there are some restrictions required, especially with respect to the leakage inductance. With inverter transistor turn-off, the drain voltage in push-pull is not clamped by the circuit topology itself. For ideal case (zero leakage), the drain voltage is clamped through the transformer coupling when the rectifier diodes are re-opened.
However, when leakage is non-zero, coupling between the primary and the secondary is not so close and the transformer acts more than an inductive load. As a result, inverter transistors receive voltage spikes and ringing at the drain voltage, usually leading to the use of MOSFETs with a higher break-down drain voltage (Figure 4-14). Due to the necessity to decrease the leakage inductance, an interleaved winding layout has to be used, as seen in Figure 4-15.
The transformer specification is presented by Table 4-6. The magnetizing inductance values are obtained from the manufacturer. The $A_L$ constant, total leakage, is obtained initially from numeric parametric simulation results, and afterwards is verified experimentally on the sample. Resistance values are measured values. Test voltages come from general standards defined for the inductive components used in SMPS. Measurements on the sample show that it is possible to achieve a relative leakage less than 0.6%.

### Table 4-6. dc/dc Transformer Specification

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetizing inductance referred to the secondary</td>
<td>2.5mH ±30-20%</td>
</tr>
<tr>
<td>Magnetizing inductance referred to the primary</td>
<td>30μH ±30-20%</td>
</tr>
<tr>
<td>Total leakage inductance referred to the secondary</td>
<td>&lt;20μH</td>
</tr>
<tr>
<td>Primary DC resistance</td>
<td>&lt;1mΩ</td>
</tr>
<tr>
<td>Secondary DC resistance</td>
<td>&lt;0.6Ω</td>
</tr>
<tr>
<td>Test Voltage secondary-to-secondary and primary-to-secondary</td>
<td>2kV AC</td>
</tr>
<tr>
<td>Test Voltage primary-to-primary</td>
<td>150V AC</td>
</tr>
</tbody>
</table>

#### 4.4.2.2 Inverter MOSFETs

As mentioned above, MOSFETs voltage rating is given by voltage spikes that can possibly occur during MOSFET switch-off. Of course it depends on the input voltage, load conditions, and transformer properties. For push-pull a number of twice the input voltage is usually sufficient. The current rating of the MOSFETs (chip size) is always a compromise because a small chip has large $R_{DS(ON)}$ that causes high conduction losses. On the other hand, a large chip has low $R_{DS(ON)}$, but the chip capacitances are higher, and, in the case of hard-switched topologies, the energy stored in the capacitances is not recovered in the switching process, but instead, energy is dissipated in the chip. This is especially the case in applications where the supply voltage is greater than 200 V.
The primary factor for chip selection are the effective drain current and the switching frequency. Then a suitable device is selected. Power loss components are calculated and compared with the designed maximum power loss per package.

Simulation results (Figure 4-12) show a value of 19.1 A (transistor and primary winding currents are the same). Dynamically, a current level as high as 50 to 60 A is observed when a load transient occurs and the regulator attempts to hold the output voltage level. Of course the transistor has to withstand such conditions for a number of milliseconds.

A couple of ON Semi’s twin NTP45N06 could be a solution. $R_{DS(ON)}$ for the transistor is 26 mΩ. If a single NTP45N06 switches the current with an effective value of 19.1 A, conduction losses are as high as 9.5 W. To lower the conduction losses and to ensure the transistor switching robustness in dynamic conditions, let’s consider the twin NTP45N06 which decrease overall conduction losses to the half (power loss per package decreases to a quarter - 2.4 W). However, the switching and the capacitance losses have to be considered, due to the increased overall chip area, and hence the overall chip capacitance.

Switching losses are given by EQ 4-26 (ref. [2]).

\[
\begin{align*}
P_{SW} &= V_{DS} \cdot (Q_{GD} + Q_{GS2}) \cdot f_{SW} \cdot \frac{I_{SW}}{I_G} \\
P_{SW} &= 24 \cdot (3nC + 15nC) \cdot 50 \times 10^3 \cdot \frac{30}{0.9} = 0.72 \text{ W}
\end{align*}
\]

Note that $V_{DS}$ can reach a level close to 60V as depending on the particular duty cycle, input voltage, and output load conditions. The same is true for $I_{SW}$ parameter, and the loss value can be impacted.

**CAUTION**

*If the output load conditions or large transformer leakage cause over voltage spikes at the drain and the maximum drain voltage is reached, the voltage is clamped by MOSFET internal avalanche process (see Figure 4-14 — fourth wave oscillation on green waveform). If the energy of the spikes is high enough, chip temperature will exceed the maximum limit and the semiconductor structure is destroyed. Please always observe the drain-to-source voltage when testing the prototype. If this is the case, increase the MOSFET voltage class or redesign the power transformer in order to decrease the leakage.*
Hardware Design

Turn-on capacitance losses $P_{\text{CAP}}$ for the NTP45N06 are given by **EQ 4-28**.

$$
P_{\text{CAP}} = f_{\text{SW}} \cdot W_{\text{CAP}} = f_{\text{SW}} \cdot \frac{1}{2} \cdot C_{\text{OSS(EFF)}} \cdot V_{DS}^2
$$

**EQ 4-28**

$$
P_{\text{CAP}} = 50 \times 10^3 \times \frac{1}{2} \cdot 380 \times 10^{-12} \cdot 60^2 = 34 \text{ mW}
$$

**EQ 4-29**

where

- $f_{\text{SW}} = \text{switching frequency}$
- $W_{\text{CAP}} = \text{capacitance energy (see ref. [1])}$
- $C_{\text{OSS(EFF)}} = \text{effective output capacity of the MOSFET (see ref. [2])}$

The sum of the switching and the capacitance losses is less than 0.8W per transistor at nominal conditions, resulting in 1.6 W for the single NTP45N06 solution and 3.2W for the twin solution. When all the loss contributions are compared, prevalence of the conduction losses is clear. The twin NTP45N06 solution results in an overall loss of 3.2W per package (the conduction component is 2.4 W, the switching component 0.8W). Therefore, the twin solution doesn’t contribute significantly to lower a converter efficiency. Power loss 3.2 W per package means moderate package utilization for TO220, with a good power loss margin.

The power losses can also be calculated by simulation of the model. **Figure 4-16** shows the MOSFET instantaneous power and energy obtained by instantaneous power integration. The average power is then calculated by the definition of the power - the energy loss referred to the switching period.

**Figure 4-16. Inverter MOSFET Power Analysis**
The use of a single transistor with a higher rated drain current is also possible, however, the copper lead utilization is rather high even though manufacturers define the value around 75 A as a limit for TO220 package leads.

4.4.2.3 Rectifier Diodes

Rated diode voltage is given by the voltage waveform applied to the diode. However, diode voltage waveforms are different from that of the MOSFETs since the rectifier diodes are placed in a different topology. As the rectifier is current-loaded there is no natural clamp for over voltage spikes at the instant of a diode reverse recovery. That is why a suitable snubber has to be implemented in order to cut-off the excess energy that could possibly overheat the diode chip by internal avalanche.

As dc/dc converter nominal output voltage is 2x390V (Figure 4-18 shows secondary voltage of the power transformer), and during dynamic conditions it can reach 2 x 420 V, the possibility of selecting the diode voltage rating is constrained. Figure 4-17 shows waveforms of the rectifier diode voltage and current. In this case, diodes with a break-down voltage of 1200V are selected.

![Figure 4-17. Rectifier Diode Voltage and Current Waveform](image_url)

When choosing the rectifier current rating, similarly as with the MOSFETs, the anode effective current and switching frequency have to be considered. Simulation results for the nominal anode effective current shows a value of 0.54 A and a 1.3 W power loss. Because the power loss is rather high for a practical usage of the DO241 package, diodes with a fully-isolated TO220 package are chosen. One possibility is to use of the Fairchild ultrafast diode FFPF05U120S with 5-A rated current, 1200 V rated voltage, and 100ns reverse recovery time, which is good enough for 50 kHz switching frequency.
4.4.2.4 Filter Chokes

A basic design consideration when implementing a filter choke is to look at the rectified current ripple. For an output current level in the range of 0.5 to 2 A, the relative ripple $r_i$ can be considered in the range of 50 to 20%. Let $r_i$ equal 30% for nominal conditions. Then the filter choke inductance value is given by

$$L = V_L \cdot \frac{\Delta T}{\Delta i} = [(V_{IN} - V_{LOSS}) \cdot p - V_{OUT}] \cdot \frac{\delta_{MAX} \cdot T}{r_i \cdot I_{OUT}} \tag{EQ 4-30}$$

$$L = [(24 - 1.6) \cdot 18 - 390] \cdot \frac{0.98 \cdot 10^{-6}}{0.3 \cdot 0.74} = 583 \, \mu H \tag{EQ 4-31}$$

where

- $V_L$ = voltage across the choke when active cycle
- $\Delta T$ = the time during active cycle
- $\Delta i$ = current ripple
- $V_{IN}$ = nominal input voltage
- $V_{LOSS}$ = voltage drop on resistive components ($R_{DS(ON)}$, transformer primary, etc.)
- $p$ = transformer primary to secondary ratio
- $V_{OUT}$ = nominal output voltage
- $\delta_{MAX}$ = maximal switching duty cycle
- $r_i$ = relative current ripple
- $I_{OUT}$ = nominal output current

Filter choke performance is analyzed by simulation, and the results (Figure 4-18) verified a good design procedure. Choke PCV2-564-02 from Coilcraft, with 560 $\mu$H inductance and 2 A saturation current, is chosen.
4.5 Power Factor Correction and Output Inverter

4.5.1 PFC Booster Operational Description

This section deals with a design of the power factor correction booster (PFC). The PFC forms the input stage of the UPS. It is a switchmode power converter, which provides an a.c. input current waveform that is sinusoidal and in phase with the line voltage. The power factor is maintained so as to be close to one.

The continuous current - boost converter topology was chosen for the PFC circuitry design, as shown in Figure 4-19. The PFC specifications are listed in Table 4-7. A power circuit consists of a current sensing transformer CT1, input inductor L505, rectifying bridge D606, power switch Q606, voltage doubler diodes D604, D608, and filtering capacitors C603, C602, C607, and C608. The PFC control algorithm implemented uses an indirect digital control approach. To decrease MCU load the input current controller is built externally.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Min.</td>
<td>80</td>
<td>V[r.m.s.]</td>
</tr>
<tr>
<td>Input Voltage Max.</td>
<td>270</td>
<td>V[r.m.s.]</td>
</tr>
<tr>
<td>Output d.c. Voltage</td>
<td>390</td>
<td>V</td>
</tr>
<tr>
<td>Output Power Nominal</td>
<td>525</td>
<td>W</td>
</tr>
<tr>
<td>Input Current Nominal</td>
<td>2.3</td>
<td>A[r.m.s]</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>30 to 60</td>
<td>kHz</td>
</tr>
</tbody>
</table>

Figure 4-18. Secondary Voltage and Rectified Current Waveforms
The output voltage level is controlled using a digital controller algorithm executed by the MCU. The MCU generates a sinusoidal reference waveform for the discrete current controller. The current controller circuit can be seen in Figure 4-20. The controller performs hysteretic current control. Comparators U606A and U606C compare the actual input current value I_IN with the upper and the low limits set by the DA1 and DA0 signals, respectively. Comparator U606B turns on and off power switch Q606 according to the U606A and U606C outputs. The UPS input current corresponds to the shape of the reference signals DA0 and DA1 generated by the MCU. The PFC operation is disabled if the PFC_EN signal is tied low by MCU control.

Alternatively (if signal DA0 is not available), the low hysteresis limit can be adjusted by the configurable voltage divider. The resulting hysteresis is then defined by the combination of resistors R664, R673, R674, and R675. The voltage divider can be configured according to the DIV1 and DIV2 signals.

**NOTE**

Selecting whether the low hysteresis limit is taken from DA0 signal or from the configurable voltage divider has to be done by resoldering the zero resistors R664 and R667. If R666 is populated, the DA0 signal is selected. If R667 is populated, the configurable divider is selected. By default R666 is populated and R667 is not.
Figure 4-20. PFC Current Controller
4.5.2 PFC Booster Design Considerations

In this section we will discuss the design considerations of the PFC booster critical components.

4.5.2.1 PFC Boost Inductor L1

The input inductor must be selected with respect to two parameters, the input current ripple and the switching frequency. It is designed for maximum input power, minimum input voltage, when the sine wave current peak is at a maximum.

The maximum input current value is then calculated from the maximum output power $P_{\text{out max}}$ and minimum input voltage $V_{\text{in min}}$. We also have to include efficiency of the boost converter. For a continuous current boost converter, the efficiency is estimated at 95%. The maximum current value is calculated as follows:

$$I_{\text{in max}} = \sqrt{2} \cdot \frac{P_{\text{out max}}}{V_{\text{in min}} \cdot \eta} = \sqrt{2} \cdot \frac{525}{184 \cdot 0.95} = 4.2 \text{A}$$  \hspace{1cm} (EQ 4-32)

If we know the input current maximum value we can calculate a current ripple. We chose the current ripple to be 15% of the input peak current. For the given peak current value it is:

$$\Delta I = I_{\text{in max}} \cdot 0.15 = 0.645 \text{A}$$  \hspace{1cm} (EQ 4-33)

When the PFC switch is turned on, the following equation has to be met:

$$L_1 \cdot \frac{\Delta I}{T_{\text{on}}} = V_{\text{in}}$$  \hspace{1cm} (EQ 4-34)

where

$L_1$ = inductance of the input boost inductor
$\Delta I$ = p-p input current ripple
$T_{\text{on}}$ = turn-on time of the PFC switch
$V_{\text{in}}$ = instantaneous input voltage value

Turn on time $T_{\text{on}}$ can be expressed from EQ 4-34 as follows:

$$T_{\text{on}} = \frac{\Delta I \cdot L_1}{V_{\text{in}}}$$  \hspace{1cm} (EQ 4-35)

When the PFC switch is turned off, the following equation has to be met:

$$L_1 \cdot \frac{-\Delta I}{T_{\text{off}}} = V_{\text{in}} - V_{\text{out}}$$  \hspace{1cm} (EQ 4-36)

where

$T_{\text{off}}$ = turn-off time of the PFC switch
$V_{\text{out}}$ = output voltage
Again, turn off time $T_{off}$ can be expressed:

$$
T_{off} = \frac{-\Delta I \cdot L_1}{V_{in} - V_{out}} \tag{EQ 4-37}
$$

Switching period $T$ equals the sum of $T_{on}$ and $T_{off}$ times:

$$
T = T_{on} + T_{off} = \frac{\Delta I \cdot L_1}{V_{in}} - \frac{\Delta I \cdot L_1}{V_{in} - V_{out}} = \frac{\Delta I \cdot L_1 \cdot V_{out}}{V_{out} \cdot V_{in} - V_{in}^2} \tag{EQ 4-38}
$$

Frequency is an inverse value of the period. The switching frequency of the PFC is then given by the formula:

$$
f_{sw} = \frac{1}{T} = \frac{V_{out} \cdot V_{in} - V_{in}^2}{\Delta I \cdot L_1 \cdot V_{out}} \tag{EQ 4-39}
$$

Switching losses of the IGBT transistor are proportional to the switching frequency. To maintain switching losses within acceptable limits we have to design the input inductor $L_1$ with respect to a maximum switching frequency. From EQ 4-39, we can calculate the level of input voltage ($V_{in}$) when the switching frequency reaches its maximum value. We get the maximum switching frequency at

$$
V_{in} = \frac{V_{out}}{2} \tag{EQ 4-40}
$$

If we substitute EQ 4-40 for EQ 4-39 we can solve the equation and find the value of the required input inductance value for the given ripple current ($\Delta I$), output voltage ($V_{out}$) and maximum switching frequency ($f_{max}$):

$$
L_1 = \frac{V_{out}}{4 \cdot \Delta I \cdot f_{max}} \tag{EQ 4-41}
$$

If we enumerate the equation for desired values we get:

$$
L_1 = \frac{390}{4 \cdot 0.645 \cdot 60 \cdot 10^3} = 2.5 \cdot 10^{-3} \text{ H} = 2.5 \text{ mH} \tag{EQ 4-42}
$$

To limit the maximum frequency at 60 kHz at ripple current 0.645 A, we choose the input PFC inductance $L_1 = 2.5$ mH.

### 4.5.2.2 L₁ Inductor Core Selection

As soon as we know the required inductance, we can proceed to select the core material and size. For the PFC application, we will consider an iron powder material.

Size of the core can be established based by an iterative process using manufacturer’s catalog data. We have chosen Micrometals as a material supplier. They offer a design software, which makes this process easier. We used this software to find the best fitting core.

In the window “PFC Boost Design Requirements” we entered the in following parameters (see Table 4-8).
We ran the calculation and got a list of suitable cores, that met our selection criteria. From the list we selected core: T175-8/90. The software calculates all important data (number of turns, wire diameter, losses, $R_{dc}$, Al, dimensions, etc.). For the selected core, the parameters are as follows:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>INDUCTANCE AT MAX CURRENT</td>
<td>2500</td>
<td>µH</td>
</tr>
<tr>
<td>MAXIMUM CURRENT</td>
<td>5</td>
<td>A</td>
</tr>
<tr>
<td>PEAK REGULATOR INPUT VOLTAGE</td>
<td>113</td>
<td>V</td>
</tr>
<tr>
<td>REGULATOR dc OUTPUT VOLTAGE</td>
<td>390</td>
<td>V</td>
</tr>
<tr>
<td>FREQUENCY</td>
<td>60</td>
<td>kHz</td>
</tr>
<tr>
<td>TEMPERATURE</td>
<td>55</td>
<td>°C</td>
</tr>
<tr>
<td>CORE SHAPE</td>
<td>TOROID</td>
<td>-</td>
</tr>
<tr>
<td>WINDING TYPE</td>
<td>FULL WINDOW</td>
<td>-</td>
</tr>
</tbody>
</table>

The core T175-8/90 meets all of our criteria, is an acceptable size, with moderate losses and good linearity.

### 4.5.2.3 dc-Bus Capacitor Design

When designing a dc-bus capacitor, we must consider its rated voltage, capacitance, size, and cost. Because there is no upper limit to the capacitance (the higher capacitance the better), we should focus on finding the possible smallest capacitance, which still meets our requirements on dc-bus voltage ripple and output voltage quality. The correct design of capacitor is very important and can significantly influence final manufacturing cost of the product. The cost of capacitor rises exponentially with its rated voltage and capacitance.
The dc-bus capacitor is a storage of energy for output power factor circuit and feeds an output inverter. The dc-bus voltage should be set above the peak at maximum r.m.s. input voltage. For input RMS voltage $V_{in} = 270$ V, the peak voltage is $V_{in \text{ peak max}} = 381$ V. To achieve good regulation of the dc-bus voltage, the dc-bus voltage should be at least 10% above the peak at nominal r.m.s. input voltage, i.e. for $V_{in \text{ nom}} = 230$ V RMS: $V_{dc \text{- bus min}} = 1.1 \times 1.41 \times 230 = 356$ V. Having $V_{in \text{ peak max}}$ and $V_{dc \text{- bus min}}$, we can determine the dc-bus nominal voltage. We chose $V_{dc \text{- bus nom}} = 390$ V.

The dc-bus capacitor voltage should at least be rated at 450 V dc.

If ac input is lost, it is desired that the dc-bus capacitor is large enough to hold up the dc-bus voltage at value $V_{dc \text{- bus hup}}$, allowing the output inverter voltage to remain within specifications for a time $T_{hup}$.

The maximum nominal output voltage is $V_{out \text{ nom}} = 230$ V RMS. The dc-bus voltage has to be higher than the output voltage peak value $V_{out \text{ peak}} = 325$ V. The hold-up time we define as a half-period of the output ac voltage frequency $T_{hup} = 10$ms. The minimum dc-bus capacitor value can calculated:

$$C_0 = \frac{I_{av} \cdot T_{hup}}{V_{dc \text{- bus nom}} - V_{out \text{ peak}}}$$  \hspace{1cm} (EQ 4-43)

where

$I_{av}$ is the average capacitor current during the drop from $V_{dc \text{- bus nom}}$ to $V_{out \text{ peak}}$.

The $I_{av}$ current can be calculated according to the formula:

$$I_{av} = \frac{2P_{out}}{\eta(V_{dc \text{- bus nom}} + V_{out \text{ peak}})}$$  \hspace{1cm} (EQ 4-44)

where

$P_{out}$ is the inverter output power

$\eta$ is the inverter efficiency

We can enumerate equation EQ 4-44 and obtain:

$$I_{av} = \frac{2 \cdot 525}{0.85(390 + 325)} = 1.728 \text{A}$$  \hspace{1cm} (EQ 4-45)

The minimum output capacitor value can be calculated if we enumerate formula EQ 4-43:

$$C_0 = \frac{1.728 \cdot 10^{-3}}{390 - 325} = 266 \cdot 10^{-6} \text{F}$$  \hspace{1cm} (EQ 4-46)

The minimum output capacitance of the dc-bus capacitor is 266$\mu$F.

The next parameter we need to know for selecting the output capacitor is the ripple current rating. The dc-bus capacitor current consists of a dc-component plus an ac-component (100/120 Hz). The dc-component flows to the load, ac-component flows into the capacitor $C_0$. The ripple current amplitude is equal to the peak load current. The ripple current can be then calculated:

$$I_{ripple} = \frac{I_{load}}{\sqrt{2}}$$  \hspace{1cm} (EQ 4-47)

The peak load current $I_{load}$ is:

$$I_{load} = \frac{P_{out}}{2 \cdot V_{dc \text{- bus nom}} \cdot \eta} = \frac{525}{2 \cdot 390 \cdot 0.85} = 0.792 \text{A}$$  \hspace{1cm} (EQ 4-48)
Ripple current is then: \( I_{\text{ripple}} = 0.792/1.41 = 0.562 \text{ A} \).

The waveform applied to the dc-bus capacitor is a near-rectangular waveform at the switching frequency. Therefore the dc-bus capacitor should have a low impedance at the switching frequency. A low-ESR electrolytic capacitor should be considered for this application.

Considering all the above requirements, we selected following dc-bus capacitor:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer</td>
<td>BC Components (Vishay)</td>
<td></td>
</tr>
<tr>
<td>Catalogue Number</td>
<td>2222 157 47331</td>
<td></td>
</tr>
<tr>
<td>Rated Capacitance</td>
<td>330</td>
<td>( \mu\text{F} )</td>
</tr>
<tr>
<td>Rated Voltage</td>
<td>450</td>
<td>V d.c.</td>
</tr>
<tr>
<td>ESR @ 100 Hz</td>
<td>300</td>
<td>m( \Omega )</td>
</tr>
<tr>
<td>Ripple Current@ 120 Hz</td>
<td>2.19</td>
<td>A</td>
</tr>
</tbody>
</table>

### 4.5.3 Output Inverter Operational Description

This section deals with the design of the output inverter of the single-phase UPS. The purpose of the output inverter is to convert dc-voltage of the dc-bus to an output single-phase sinusoidal voltage of the required amplitude and frequency.

The topology of the inverter circuitry is shown in Figure 4-21. The power circuit consists of IGBT power switches Q605 and Q608, which are connected across dc-bus capacitors C602, C608. An emitter terminal of Q605 and a collector terminal of Q608 are connected to a sinusoidal filter (inductor L506 and a capacitor C605). Output of the sinusoidal filter is then connected to the by-pass relay RE2 and EMC filter (L205, C604, C602). Output relays RE1, RE3, connect the inverter output to output terminals of the UPS. The nominal specifications of the output inverter are listed in the Table 4-11.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Min.</td>
<td>2x340</td>
<td>V[d.c.]</td>
</tr>
<tr>
<td>Input Voltage Max.</td>
<td>2x430</td>
<td>V[d.c.]</td>
</tr>
<tr>
<td>Output a.c. Voltage</td>
<td>80 - 270</td>
<td>V [r.m.s.]</td>
</tr>
<tr>
<td>Output Apparent Power Nominal(^{1})</td>
<td>750</td>
<td>VA</td>
</tr>
<tr>
<td>Output Current Nominal</td>
<td>3.3</td>
<td>A[r.m.s]</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>20</td>
<td>kHz</td>
</tr>
</tbody>
</table>

\(^{1}\) Nominal output apparent power for nominal output voltage 230 V r.m.s.
Figure 4-21. Output Inverter Power Circuit
The power IGBTs Q605 and Q608 switch in a complementary manner (if Q605 is on, Q608 is off, and vice versa). Using the power IGBTs, the dc-bus voltage is pulse-width modulated at 20kHz switching frequency to obtain an output voltage with a low frequency a.c. component (50/60 Hz). The junction of C602 and C608 is a zero-volts reference for the generated output waveform. The junction of the capacitors is galvanically connected to the mains N-terminal and is labelled as system ground.

Switching pulses to gates Q605 and Q608 are generated by the dual IGBT gate opto-drive HCPL-315J (U615). The opto-drive provides the circuitry with galvanic isolation between the MCU and each of the IGBTs. Its topology is shown in the Figure 4-22. The IGBT gates are floating during the inverter operation in a voltage range +/- 430 V dc. Each channel of the dual opto-drive IC is supplied from a galvanically isolated voltage supply of +15V dc.

**Figure 4-22. Inverter IGBT Gate Drive Circuitry**

The by-pass relay RE2 connects the UPS output to either the inverter or the mains voltage.

The relays RE1 and RE3 connect the UPS output socket banks to the output voltage.

A current transformer CT2 is put into the output current path. Together with current-to-voltage converter circuitry, it makes up the sensing circuitry of the output load current.

**NOTE**

*Please note that during operation, the voltage on the power IGBTs is a sum of the voltages on the dc-bus capacitors, i.e., it can reach up to 2 x 430 V = 960 V! The IGBTs must be rated for a collector-emitter voltage of 1200 V.*
4.5.4 Output Inverter Design Considerations

In this section we will discuss the design considerations of the critical components of the output inverter.

The sinusoidal output filter is a low-pass LC-filter consisting of an inductor \( L_{506} \) and a capacitor \( C_{605} \). The resonant frequency of the circuit has to be selected with respect to the output voltage control loop. Based on the Simulink simulation results we have selected a resonant frequency in the range: 600 to 900 Hz.

Having the resonant frequency we are able to select values of the inductor and capacitor. To achieve the required resonant frequency of the filter we have plenty of variants of \( L \) and \( C \) distribution. The values of the components have to be selected with consideration of their size, cost and availability. Considering the components available in the market, we have chosen following combination:

- \( L_{506} = 5 \) mH
- \( C_{605} = 6.8 \) \( \mu \)F

The resonant frequency of such a circuit is 863 Hz and falls in our range.

4.5.4.1 \( C_{605} \) Capacitor Selection

The capacitor parameters have to fulfil safety requirements for rated ac voltage. Low ESR and ESL parameters are required to achieve a low output voltage ripple. For the output sinusoidal filter we selected MKP 338 4 X2 capacitor from Vishay BC components. See Table 4-12.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance</td>
<td>6.8 ( \mu )F</td>
</tr>
<tr>
<td>Capacitance tolerance</td>
<td>20%</td>
</tr>
<tr>
<td>Rated (ac) voltage, 50 to 60 Hz</td>
<td>300V</td>
</tr>
<tr>
<td>Rated (dc) voltage</td>
<td>630V</td>
</tr>
<tr>
<td>Rated temperature</td>
<td>105°C</td>
</tr>
<tr>
<td>Safety class</td>
<td>X2; across the line</td>
</tr>
</tbody>
</table>

4.5.4.2 \( L_{506} \) Inductor Core Selection

As soon as we know the required inductance, we can proceed to select the core material and size. Because the inductor current contains a high frequency ripple, we will consider an iron-powder core.

Size of the core can be established by an iterative process using the manufacturer’s catalog data. We have chosen Micrometals as the material supplier. Again as with the PFC inductor design, we used the Micrometals software to find the best fitting core.

For the design of the output filter inductor, we can use either “dc biased” design or “PFC boost”. The calculations of both are similar, however, the “PFC Boost” calculations account for a periodic change to the switching duty-cycle. We can thus more accurately represent the losses in the inductor core. Therefore we selected “PFC Boost” design. In the parameter window of the design, we entered the parameters shown in Table 4-13.
Note that we swapped the input and output peak voltage values in the design parameters. In a real inverter, the dc voltage is the input parameter and the ac voltage is the output parameter. To make an analogy with PFC, we have to swap these parameters in the input table.

We ran the calculation and got a list of suitable cores that met our selection criteria. From the list we selected core: T200-30B. The software calculates all important data (number of turns, wire diameter, losses, $R_{dc}$, $A_l$, dimensions, etc.). For the selected core, the parameters are as follows:

**Table 4-13. Output Filter Inductor Parameters**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance at max current</td>
<td>5000</td>
<td>µH</td>
</tr>
<tr>
<td>Maximum current</td>
<td>4.6</td>
<td>A</td>
</tr>
<tr>
<td>Peak regulator input voltage</td>
<td>340</td>
<td>V</td>
</tr>
<tr>
<td>Regulator dc output voltage</td>
<td>400</td>
<td>V</td>
</tr>
<tr>
<td>Frequency</td>
<td>20</td>
<td>kHz</td>
</tr>
<tr>
<td>Temperature</td>
<td>55</td>
<td>°C</td>
</tr>
<tr>
<td>Core shape</td>
<td>Toroid</td>
<td>-</td>
</tr>
<tr>
<td>Winding type</td>
<td>Full window</td>
<td>-</td>
</tr>
</tbody>
</table>

**NOTE**

*Note that we swapped the input and output peak voltage values in the design parameters. In a real inverter, the dc voltage is the input parameter and the ac voltage is the output parameter. To make an analogy with PFC, we have to swap these parameters in the input table.*

Table 4-14. Design Parameters for Core P/N: T175-8/90

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_l$</td>
<td>51</td>
<td>nH</td>
</tr>
<tr>
<td>Turns</td>
<td>388</td>
<td>-</td>
</tr>
<tr>
<td>Wire</td>
<td>1.00</td>
<td>MM</td>
</tr>
<tr>
<td>Fill</td>
<td>38.5</td>
<td>%</td>
</tr>
<tr>
<td>$R_{dc}$</td>
<td>0.8868</td>
<td>Ohms</td>
</tr>
<tr>
<td>Core loss</td>
<td>1.46</td>
<td>W</td>
</tr>
<tr>
<td>Cu loss</td>
<td>9.38</td>
<td>W</td>
</tr>
<tr>
<td>Temperature rise</td>
<td>46.4</td>
<td>°C</td>
</tr>
</tbody>
</table>

The core T200-30B meets all of our criteria, is an acceptable size, with moderate losses and low price.
5.1 Introduction
This section describes the design of the software blocks for the UPS. The software is described in terms of:

- Data flow
- Main software flowchart
- State diagram

For more information on the control technique used, see Chapter 3 UPS Control.

5.2 Data Flow
The control algorithm obtains values from the user interface and sensors, processes them, and generates PWM signals for the dc/dc step-up converter, output inverter, and sine wave reference for PFC, as can be seen on the data flow analysis shown in Figure 5-1.

5.2.1 Software Variables and Defined Constants
Important system variables, named in the data flow, are listed in Table 5-1. The table includes the name, range used, and representation in real quantities.
Figure 5-1. Main Data Flow
<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>&lt;Range&gt;; [Scale]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>amp_ControllerPar</td>
<td>Structure</td>
<td>-</td>
<td>PI controller parameters for RMS correction</td>
</tr>
<tr>
<td>amplitude_correction</td>
<td>U16</td>
<td>&lt;0, 39936&gt;; [0V, 400V]</td>
<td>output of RMS correction</td>
</tr>
<tr>
<td>amplitude_ref</td>
<td>U16</td>
<td>&lt;0, 39936&gt;; [0V, 400V]</td>
<td>required amplitude of output sine wave</td>
</tr>
<tr>
<td>appState</td>
<td>enum</td>
<td>-</td>
<td>state of application state machine</td>
</tr>
<tr>
<td>BatState</td>
<td>enum</td>
<td>-</td>
<td>state of battery charger</td>
</tr>
<tr>
<td>counter_actual</td>
<td>U16</td>
<td>&lt;0.5580&gt;; [0 s, 7.14 ms (70 Hz)]</td>
<td>period of input voltage zero crossing</td>
</tr>
<tr>
<td>dcdc_duty</td>
<td>U16</td>
<td>&lt;0, 121&gt;; [0%, 96.8%]</td>
<td>duty cycle of dc/dc step-up converter</td>
</tr>
<tr>
<td>i_bat</td>
<td>S16</td>
<td>&lt;0, 1023&gt;; [0 A, 2.34 A]</td>
<td>battery charging current</td>
</tr>
<tr>
<td>i_out</td>
<td>S16</td>
<td>&lt;-32768, 32767&gt;; [-13 A, 13 A]</td>
<td>actual output current</td>
</tr>
<tr>
<td>i_out_rms</td>
<td>S16</td>
<td>&lt;-32768, 32767&gt;; [-13 A, 13 A]</td>
<td>RMS value of output current</td>
</tr>
<tr>
<td>pfc_ref_h</td>
<td>U8</td>
<td>&lt;0, 152&gt;; [0 A, 5 A]</td>
<td>required actual input (PFC) current</td>
</tr>
<tr>
<td>phase_diff</td>
<td>S16</td>
<td>&lt;-32768, 32767&gt;; [-180º, 180º]</td>
<td>phase difference between expected and actual phase of PLL</td>
</tr>
<tr>
<td>phase_measured</td>
<td>S16</td>
<td>&lt;-32768, 32767&gt;; [-180º, 180º]</td>
<td>calculated phase</td>
</tr>
<tr>
<td>phase_out</td>
<td>S16</td>
<td>&lt;-32768, 32767&gt;; [-180º, 180º]</td>
<td>actual phase of generated output voltage</td>
</tr>
<tr>
<td>phase_out_inc</td>
<td>U16</td>
<td>&lt;33554, 58720&gt;; [40 Hz, 70 Hz]</td>
<td>increment to sine wave table (output voltage)</td>
</tr>
<tr>
<td>phase_pfc</td>
<td>S16</td>
<td>&lt;-32768, 32767&gt;; [-180º, 180º]</td>
<td>actual phase of input voltage calculated by PLL</td>
</tr>
<tr>
<td>PWMB_duty_cycle</td>
<td>U16</td>
<td>&lt;0, 625&gt;; [100%, 100%]</td>
<td>duty cycle of output inverter</td>
</tr>
<tr>
<td>PWMC_duty_cycle</td>
<td>U16</td>
<td>&lt;0, 121&gt;; [0%, 96.8%]</td>
<td>duty cycle of dc/dc step-up converter</td>
</tr>
<tr>
<td>temperature</td>
<td>U16</td>
<td>&lt;0, 205&gt;; [0 ºC, 100 ºC]</td>
<td>temperature of power stage heatsink</td>
</tr>
<tr>
<td>v_bat</td>
<td>U16</td>
<td>&lt;0, 1023&gt;; [0 V, 39 V]</td>
<td>battery voltage</td>
</tr>
<tr>
<td>v_dcb[]</td>
<td>U16</td>
<td>&lt;0, 1023&gt;; [0 V, 450 V]</td>
<td>dc bus voltage</td>
</tr>
<tr>
<td>v_dcdcControllerPar</td>
<td>Structure</td>
<td>-</td>
<td>PI controller parameters for dc/dc controller</td>
</tr>
<tr>
<td>v_in</td>
<td>U16</td>
<td>&lt;0, 1023&gt;; [0 V, 324 V]</td>
<td>RMS value of input voltage</td>
</tr>
<tr>
<td>v_out</td>
<td>S16</td>
<td>&lt;-19968, 19968&gt;; [-400 V, 400 V]</td>
<td>actual output voltage</td>
</tr>
<tr>
<td>v_out_freq_detect</td>
<td>U16</td>
<td>&lt;33554, 58720&gt;; [40 Hz, 70 Hz]</td>
<td>detected input frequency</td>
</tr>
<tr>
<td>v_out_rms</td>
<td>U16</td>
<td>&lt;-19968, 19968&gt;; [-400 V, 400 V]</td>
<td>RMS value of output voltage</td>
</tr>
<tr>
<td>v_pfcControllerPar</td>
<td>Structure</td>
<td>-</td>
<td>PI controller parameters for PFC controller</td>
</tr>
<tr>
<td>v_sine_ref</td>
<td>S16</td>
<td>&lt;-19968, 19968&gt;; [-400 V, 400 V]</td>
<td>required value of output voltage (sine wave reference including amplitude correction)</td>
</tr>
</tbody>
</table>

Type: S8 = signed 8-bit, U8 = unsigned 8-bit, S16 = signed 16-bit, U16 = unsigned 16-bit.
5.2.2 Process PLL Algorithm

The PLL algorithm synchronizes the pointer to the PFC sine wave reference with the input line voltage. The algorithm uses the variable `counter_actual` as an input and calculates the `phase_pfc`, `phase_pfc_inc`, `phase_out` and `phase_out_inc`. The variables relating to the output inverter are generated if the output is synchronized with the output.

5.2.3 Process RMS Correction

Because the output inverter PID controller is not able to keep a constant RMS value of output voltage due to slight or missing integral part of the controller, the RMS correction must be calculated. The RMS controller compares the actual RMS value `v_out_rms` with the required RMS value calculated from `amplitude_ref`. The output of PI controller is correction to the amplitude, stored in `amplitude_correction`.

5.2.4 Process Mains Line Detection

This process sets the mains line system to 230 V, 50 Hz or 115 V, 60 Hz according to state of START/STOP switch on the MC9S12E128 controller board. The detected values `amplitude_ref` and `v_out_freq_detected` are used for the output inverter to generate the correct output and for the PFC PLL to determine that the PLL algorithm is synchronized.

5.2.5 Process Ramp

The ramp process changes an input value in a time period with a predefined slope. A different ramp can be defined for a rising and falling slope.

5.2.6 Process Sine Wave Reference

The sine wave reference process generates the sine wave reference waveform `v_sin_ref` based on the actual phase `phase_out`, phase increment corresponding to the generated frequency `phase_out_inc`, and amplitude `amplitude_ref + amplitude_correction`.

5.2.7 Process Button Processing

The button processing reads the status of the ON/OFF and BYPASS buttons. It recognizes a short and long push. The results are saved in variable `buttonStatus`.

5.2.8 Process LED Processing

The process handles the LEDs on the user interface. Each LED can be switched on, off, or to flash. The LED status bar works in two modes. In output power mode, the status bar displays the actual output power. In battery mode it shows remaining battery capacity.

5.2.9 Process Application State Machine

This process provides the state machine of UPS. The state machine defines the following states:
- Init
- Standby on battery
- Standby on line
- Run on battery
After **RESET**, the state machine enters into the **Standby on battery** state if the mains line is available. Then if the user pushes the ON/OFF button, the state machine continues on to the **Run on line** state. During mains line failure, the state machine goes to the **Run on battery** state. The state machine stays there until the batteries are discharged, the user switches the UPS off, or the main line is restored. If the batteries are discharged the state machine goes to the **Standby on battery** state. If the state machine stays in this state one minute, the UPS is switched off (**UPS state**) to avoid total discharge of the batteries. In the case of some fault, the state machine goes into the **Error** state.

If the state machine goes from one to another state, a respective transition function is called.

### 5.2.10 Process PFC Control

The PFC control process consists of the PI controller, which controls the dc bus voltage \( v_{dcb}[] \) to the required value \( v_{dcb\_req} (v_{dcb\_req\_rmp}) \). The result defines the amplitude of the input current \( i_{n\_ref} \).
5.2.11 Process Sine Wave Reference (PFC)

This process generates a rectified sine wave waveform based on the required amplitude $i_{n\_ref}$, actual phase $\text{phase\_pfc}$, and the required frequency $\text{phase\_pfc\_inc}$. The result $\text{pfc\_ref\_h}$ is sent to the D/A converter and is used as the reference for the external current controller.

5.2.12 Process dc Bus Scaling

The scaling process calculates the correction constant $\text{PWM\_to\_DCB\_scale}$ for inverter duty cycle. The duty cycle, which outputs from the PID controller, is related to constant dc bus voltage. If the actual dc bus is different, the duty cycle has to be recalculated to the actual dc bus. For example, if the output duty cycle is 50% (195 V) for 390 V of dc bus voltage and the actual dc bus voltage is equal to 380 V, the resultant duty cycle has to be recalculated to 51.3% to maintain 195 V.

5.2.13 Process dc/dc Step-Up Control

The process is similar to the PFC control process. The input value is $v\_\text{dcdc\_req}$ ($v\_\text{dcdc\_req\_rmp}$) and the result is $\text{PWM\_duty\_cycle}$.

5.2.14 Process Inverter Control

The inverter control process performs PID controller including feed forward technique. The inputs are $v\_\text{sin\_ref}$, $v\_\text{out}$, and $\text{PWM\_to\_DCB\_scale}$, and the output is the duty cycle $\text{PWM\_duty\_cycle}$.

5.2.15 Process Battery Charge Control

The battery charger control process charges the batteries. The charging current $i\_\text{bat}$ and battery voltage $v\_\text{bat}$ are read, and according to the actual battery current, the state of the charging algorithm $\text{BatState}$ is set to BULK CHARGE MODE, ABSORPTION MODE, or FLOAT MODE.

5.3 Main Software Flowchart

The software is written in C language using Metrowerks CodeWarrior software. Some time-critical parts such as sine wave generation and arithmetical functions are written in assembler.

The software consists of the following parts:

- Initialization of peripherals and variables
- Background group
- 5 periodic interrupts (2 x 50 $\mu$s, 1 x 1 ms, 1 x 10 (8.3) ms, 1 x 50 ms)
- 3 event interrupts (PMF faults, LVI, SCI)

5.3.1 Initialization of Peripherals and Variables

After RESET, the program goes into the initialization routine. The routine initializes the following peripherals:

- PLL
- I/O pins
- Analog to digital converter
- Digital to analog converter
- Pulse-width modulator with fault protection
- Timer 0
- Pulse-width modulator
- Voltage regulator

Subsequently, the communication with the PC is initialized, and the program variables are set to default values.

Then the program enters the never-ending loop providing the application state machine (see main function listing below).

```c
void main ()
{
    InitPeripherals();
    PCMaster_Config();
    EnableInterrupts; /* enable interrupts to make this routine
                    interruptible
                    (defined int PCMaster-S12.h) */
    PCMasterInit(); // init PCMaster functions
    InitVariables();
    while(1)
    {
        appStateFcn[appState]();
        FanControl();
    }
}
```

The structure of the background loop can also be seen in Figure 5-3.
5.3.2 Periodic Interrupts

The software uses five periodic interrupts. They are:
- PMF reload interrupt (called every 50 μs)
- ATD conversion complete interrupt (called every 50 μs)
- TIM0 CH4 input capture interrupt (called every 8.3 or 10 ms)
- TIM0 CH5 output compare interrupt (called every 1 ms)
- TIM0 CH6 output compare interrupt (called every 50 ms)

5.3.2.1 PMF Reload Interrupt

The PMF Reload Interrupt is part of the UPS main control loop. The source of the interrupt is a reload event of counter B (output inverter). The structure of the interrupt can be seen on Figure 5-4.

Figure 5-4. Structure of PMF Interrupt

The interrupt starts by reading a slow ATD conversion. A slow ATD conversion means that the quantities are not converted every 50 μs. There is a table which defines the order of quantities to be converted. The results of a slow ATD conversion are ready from previous interrupt.

After saving the conversion results, a fast ATD conversion is set and started. A fast ATD conversion means that the quantities are converted every interrupt (50 μs). The output voltage and current are sensed in the fast ATD conversion.
While the fast ATD conversion is running the following tasks are performed:
- Detection of missing zero crossing on the input line
- Detection of input voltage polarity
- RMS value calculation and output power calculation (multiplication and addition)
- Generation of rectified sine waveform for the PFC
- Generation of sine wave reference for the output inverter

The execution time for these tasks is shorter than the conversion time in a fast ATD conversion.

### 5.3.2.2 ATD Conversion Complete Interrupt

As soon as the fast conversion is completed and the PMF reload interrupt executed, the ATD conversion complete interrupt is called. This interrupt performs the inverter control and starts the next slow ATD conversion (see Figure 5-5). Because this interrupt is bounded by the PMF reload interrupt, the execution period is also 50 µs.

Both interrupts, together with the TIM0 CH5 output compare interrupt, comprise the main part of the UPS control algorithm. The PMF reload and ATD conversion complete interrupts have the highest priority and are uninterruptible.

![Figure 5-5. Structure of ATD Conversion Complete Interrupt](image)

### 5.3.2.3 TIM0 CH4 Input Capture Interrupt

The source of this interrupt is a zero crossing on the input voltage. So the interrupt is executed every 8.3 ms or 10 ms. The interrupt performs a phase locked loop algorithm, which synchronizes the generation of PFC and output inverter sine wave references with the input voltage.
5.3.2.4 TIM0 CH5 Output Compare Interrupt

The source of this interrupt is the output compare event, set to generate event every 1 ms. This interrupt comprises the second part of the control algorithm. The structure of the interrupt is shown in Figure 5-7.

The interrupt performs following tasks:

- Voltage control loop of the PFC
- dc/dc step-up converter control loop
- Filtering and scaling of analog values measured in the slow ATD conversion
- finishing the RMS and output power calculations (multiplication by constant and square root)
- RMS correction algorithm

This routine has a lower priority and can be interrupted by the PMF reload and ATD complete interrupts.
5.3.2.5 TIM0 CH6 Output Compare Interrupt

The last periodic interrupt is called every 50 ms. The time base is derived from TIM0 CH6 output compare event, which is set to generate this period. The interrupt performs background tasks which require periodic execution but with a very low priority. The tasks are:

- Software timers
- User interface handling (buttons, LED diodes)
- Battery charger algorithm

![TIM0 CH6 Output Compare Interrupt Diagram](image)

**Figure 5-8. Structure of TIM0 CH6 Output Compare Interrupt**

5.3.3 Event Interrupts

The event interrupts are called on an event. The UPS application uses following event interrupts:

- SCI interrupt (performing the communication with PC)
- PMF fault interrupt
- Voltage regulator — low voltage inhibit interrupt

5.3.4 Interrupt Time Execution and MCU Load Estimation

The time execution of periodic interrupts was measured by oscilloscope. The result can be seen in **Figure 5-9**.
Figure 5-9. CPU Load of UPS Application

Trace 1 (blue) represents a PMF reload interrupt; Trace 2 (cyan) is an ATD complete interrupt; Trace 3 shows 1 ms interrupt; Trace 4 (green) is 50 ms. The total MCU load is 65.16%. The execution time of each interrupt can be seen in Table 5-2, and the size code in Table 5-3.

Table 5-2. Execution Time of Periodic Interrupts

<table>
<thead>
<tr>
<th>Name</th>
<th>Execution Period</th>
<th>Execution Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMF reload interrupt</td>
<td>50 µs</td>
<td>15.8 µs</td>
</tr>
<tr>
<td>ATD conversion complete interrupt</td>
<td>50 µs</td>
<td>14.2 µs</td>
</tr>
<tr>
<td>TIM0 CH4 input capture interrupt</td>
<td>8.3 ms or 10 ms</td>
<td>7.8 µs</td>
</tr>
<tr>
<td>TIM0 CH5 output compare interrupt</td>
<td>1 ms</td>
<td>50 µs</td>
</tr>
<tr>
<td>TIM0 CH6 output compare interrupt</td>
<td>1 ms</td>
<td>35.8 µs</td>
</tr>
</tbody>
</table>

Table 5-3. Size of UPS Application Code

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>Size in Bytes</th>
</tr>
</thead>
<tbody>
<tr>
<td>FLASH</td>
<td>10087</td>
</tr>
<tr>
<td>RAM</td>
<td>2502</td>
</tr>
<tr>
<td>Stack</td>
<td>512</td>
</tr>
</tbody>
</table>
5.4 Software Constant Calculations

This section describes the calculation of some software constants from real values to software implementation.

5.4.1 PI and PID Controller Constants

Because the MCU works with integer arithmetic only each constant $K_{REAL}$ in the real system is expressed in the software as:

$$K_{REAL} = \frac{\text{GAIN}}{2^{(16-\text{SCALE})}}$$  \hspace{1cm} (EQ 5-1)

To keep the maximal precision of calculation, the SCALE should be set in order to push the GAIN into the upper half of the variable range.

Example:

Let's convert a constant 25 in U16 representation. The upper half of the U16 range is from 32768 to 65536. The get this constant to optimal range we set the SCALE to 5. Then the GAIN = 25 .

$$2^{(16-5)} = 51200.$$  

**NOTE**

*Note that the SCALE is shared for all constants in the PI/PID controller. So in case of a highly different order in the constants, a compromise has to be made.*

The controller implementation is explained in 3.1.5 PI and PID Controller. From EQ 3-7 results, the proportional constant is equal to the gain of the system.

The integral constant of the controller can be expressed as:

$$\frac{K_h}{T_I}$$  \hspace{1cm} (EQ 5-2)

where

- $T_I$ = Integral time constant
- $h$ = Sampling time
- $K$ = Controller gain

See EQ 3-8. The derivative constants are defined as:

$$kd_1 = \frac{T_D}{T_D + Nh}$$  \hspace{1cm} (EQ 5-3)

$$kd_2 = \frac{KT_D N}{T_D + Nh}$$  \hspace{1cm} (EQ 5-4)
**Software Design**

where

\[
\begin{align*}
    h & = \text{Sampling time} \\
    T_D & = \text{Derivative time constant} \\
    N & = \text{Filter constant}
\end{align*}
\]

**NOTE**

The proportional constant of the output inverter controller is called \( q_1 \) in the software.

**Example:**

Let's have constants for the PFC controller. The PFC uses the PI controller, where the controller gain \( K(P) = 100 \) and Integral time constant \( T_I = 0.0016 \) s. The controller is calculated every 1 ms.

From EQ 5-2 we can calculate integral constant as:

\[
\frac{100 \cdot 1 \cdot 10^{-3}}{0.0016} = 6.25.
\]

Since the scale is common for both constants, we choose \( \text{SCALE} = 8 \). Then we get a proportional gain \( 100 \cdot 2^{(16-8)} = 25600 \) and an integral gain \( 6.25 \cdot 2^{(16-8)} = 1600 \). In the source code we can see:

```c
#define PFC_P_GAIN_BASE 25600
#define PFC_I_GAIN_BASE 1600
#define PFC_SCALE 8
```
Chapter 6
Tests and Measurements

6.1 Test Equipment
All tests were done using the following equipment:
- 2x multimeter 34401A, Hewlett Packard
- Scope TDS3014B, Tektronix
- 3-phase precision power meter LMG 310, Zimmer Electronic Systems

6.2 Load Parameters
The parameters were measured for both linear and non-linear loads. The loads were calculated according to standard IEC 62040-1. The reference load was calculated for a nominal output power of 750 VA. The parameters of the loads are:
- Linear load: R = 100 Ω
- Non-linear load: R = 160 W, Rs = 2.8 W, C = 780 mF (see Figure 6-1)

Figure 6-1. Non-Linear Load
6.3 Test Results

6.3.1 Overall Efficiency at Linear Load

The total efficiency at a linear load is 91%. See Figure 6-2. The picture shows the display of 3-phase precision power meter indicating the input power (P1), output power (P2), losses (LOSS) and calculated efficiency (EFF).

![Figure 6-2. Overall Efficiency at Linear Load](image)

Figure 6-3. Output Voltage and Current at Linear Load
6.3.2 Overall Efficiency at Non-linear Load

The total efficiency at a non-linear load is 90%. See Figure 6-4.

![Image of Overall Efficiency at Non-linear Load](image)

**Figure 6-4. Overall Efficiency at Non-linear Load**

![Image of Output Voltage and Current at Non-linear Load](image)

**Figure 6-5. Output Voltage and Current at Non-linear Load**
6.3.3 Output Frequency Measurement

The next two pictures show the generation of output frequency. The left multimeter shows input frequency, and the right one shows output frequency. Figure 6-6 shows the synchronized output with input. Figure 6-7 shows a free running mode. In this case the precision of the output frequency is given by the precision of the MCU crystal.

Figure 6-6. Output Frequency in Synchronized Mode

Figure 6-7. Output Frequency in Free-running Mode
6.3.4 Output Voltage THD

Output voltage THD was measured for three cases:
- Without load: THD = 0.4%
- With full linear load: THD = 1%
- With full non-linear load: THD = 5%

The next two pictures show details of output voltage and current at a non-linear load.

Figure 6-8. Output Voltage and Current at Non-linear Load — Detail

Figure 6-9. Output Voltage and Current at Non-linear Load
6.3.5 Power Factor Measurement

The power factor measured can be seen in Figure 6-10. The figure shows input voltage $U_3$, input current $I_3$, and power factor $\lambda_3$.

![Figure 6-10. Power Factor Measurement](image)

6.3.6 Response on Step Load

The following four pictures show the response of the output controller a on step load from 20% to 100%, and vice versa, for a linear load.
Figure 6-11. Load Step from 20% to 100%

Figure 6-12. Load Step from 20% to 100% — Detail
Figure 6-13. Load Step from 100% to 20%

Figure 6-14. Load Step from 100% to 20% — Detail
6.3.7 Summary
All measured parameters are summarized in Table 6-1

Table 6-1. Summary of Measured Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Linear</td>
</tr>
<tr>
<td>Efficiency</td>
<td>91%</td>
</tr>
<tr>
<td>Output voltage THD without load</td>
<td>0.4%</td>
</tr>
<tr>
<td>Output voltage THD</td>
<td>1%</td>
</tr>
<tr>
<td>Power factor</td>
<td>0.99</td>
</tr>
<tr>
<td>Precision of generated frequency</td>
<td>&lt; 0.01%</td>
</tr>
</tbody>
</table>
Chapter 7
System Set-Up and Operation

**WARNING**
This application operates in an environment that includes dangerous voltages. The application includes batteries and dangerous voltage may appear even if the application is not connected to the mains line. An isolating transformer should be used during debugging. If an isolating transformer is not used, power stage grounds and oscilloscope grounds will be at different potentials, unless the oscilloscope is floating. Note that probe grounds, such as in the case of a floating oscilloscope, are subject to dangerous voltages. Take note of the following points and recommendations

- Switch off the high-voltage supply before moving scope probes or making connections.
- Avoid inadvertently touching live parts, and use plastic covers where possible.
- When the high voltage is applied, using only one hand to operate the test setup will reduce the possibility of electrical shock.
- Avoid using the application in laboratory environments that have grounded tables or chairs.
- Wear safety glasses, avoid ties and jewelry, use shields, and make use of personnel trained in high-voltage laboratory techniques.
- The power module heatsink can reach temperatures hot enough to cause burns.
- When powering down, due to storage in the bus capacitors, dangerous voltages are present until the power-on LED is off.

7.1 Hardware Setup
The UPS demo is mounted into a metal case which provides safe operation. The case cover is made from transparent plastic, which allows the UPS construction to be seen (see Figure 7-1).
Figure 7-1. UPS Demo

WARNING

Do not touch any part of the board inside the metal case regardless of whether the UPS is running from mains line or batteries. There is a high risk of electric shock caused by high voltage, which may cause serious injury or death.

To prepare the UPS for operation, follow these steps:

1. Connect the power supply cable to the INPUT LINE socket.
2. Connect the load supply cable to any OUTPUT SECTION socket. Be sure that the load power is within the limit of the UPS demo.
3. In the case of remote operation from a PC, connect a serial cable between the PC and the J2 connector of the UPS (on the right-hand side in Figure 7-3 and Figure 7-5).
4. Switch MAINS INPUT LINE switch ON.

If the mains line is available, the UPS will go into standby on-line mode. In this mode, the MCU works and the batteries are charged, but the output is still switched off.

5. In the case of remote operation, run the FreeMaster software on the PC and load the project file, UPS.pmp.

The UPS is ready for operation.
7.1.1 Setting of Mains Line System

Because the UPS can not detect the mains line system if it starts to run from batteries, the system can be predefined by the START/STOP switch on the MC9S12E128 controller board. If the switch is in the RUN position, the UPS generates outputs 230 V, 50 Hz. In STOP position, the UPS generates 115 V, 60 Hz.
7.2 Software Setup

7.2.1 Application Software Files

The application software files are:
- \software\UPS\OnlineUPS\on_line_ups.mcp, application project file
- \software\UPS\OnlineUPS\sources\main.c, main program
- \software\UPS\OnlineUPS\sources\main.h, header file for main code
- \software\UPS\OnlineUPS\sources\PCMaster.c, library of FreeMaster functions
- \software\UPS\OnlineUPS\sources\PCMaster.h, library of FreeMaster functions definitions file
- \software\UPS\OnlineUPS\sources\PCMasterConfig.h, configuration file for FreeMaster
- \software\UPS\OnlineUPS\sources\projectglobals.h, global definitions file of HCS12 stationary
- \software\UPS\OnlineUPS\sources\projectvectors.c, source file of interrupt routines
- \software\UPS\OnlineUPS\sources\projectvectors.h, header file for interrupt routines
- \software\algorithms\sin.asm, library with sine wave generation functions
- \software\algorithms\sin.h, header file for sine wave generation functions
- \software\algorithms\sinlut.asm, sinus look up table for sine wave generation functions
- \software\algorithms\upsmath.asm, library of mathematical functions written in assembler
- \software\algorithms\upsmath.c, library of mathematical functions written in C language
- \software\algorithms\upsmath.h, header file for library of mathematical functions

7.2.2 Application PC Master Software Control Files

The application PC master software control files are:
- \software\UPS\OnlineUPS\PCMaster\UPS.pmp, PC master software project file
- \software\UPS\OnlineUPS\PCMaster\source, directory with PC master software control page files
7.2.3 Application Build

To build the online UPS application, open the on_line_ups.mcp project file and execute the *Make* command, as shown in Figure 7-4. This will build and link the application with all the required Metrowerks libraries.

![Figure 7-4. Execute Make Command](image-url)
7.2.4 Programming the MCU

Because the UPS power supply is controlled by the MCU, the following sequence must be used to program the MCU:

1. Switch the UPS OFF by the ON/OFF switch
2. Switch the MAINS LINE switch to OFF
3. Wait one minute until the UPS has totally switched off
4. Disconnect the power supply cable from the socket
5. Remove the transparent plastic cover
6. Disconnect the cable from J4 on the user interface
7. Connect a BDM cable to the MC9S12E128 controller board
8. Connect the cable to any test point named GND on the UPS power stage (e.g., TP206)
9. Load the code to the MCU
10. Remove the cable from GND test point and wait until the UPS has totally switched off
11. Connect the cable back to J4 on the user interface
12. Re-install the transparent plastic cover

**WARNING**
*The BDM connector is not galvanically isolated. Therefore, be sure that the UPS is disconnected from the mains line during programming.*

7.3 Application Control

The UPS can be controlled by the MAINS LINE switch (Figure 7-2) and by the two ON/OFF or BYPASS buttons. The status of the UPS is indicated by four LEDs and an LED bar graph.

7.3.1 On-line Operation

If the mains line is available and the UPS is set up as is described in 7.1 Hardware Setup, the UPS is in standby on-line mode. To switch the UPS on, quickly push the ON/OFF button. As soon as the button is released the UPS goes into run on-line mode. All UPS outputs are active and the UPS supplies the load. The run on-line mode is indicated by the green status LED. The actual load is indicated by LED bar graph. Optionally, a bypass can be activated by quickly pushing the BYPASS button. In bypass mode the load is connected directly to the mains line. The bypass mode is indicated by the yellow LED.
In the case of a mains line failure, the UPS automatically goes into run on battery mode. If the UPS is in bypass mode at the moment of the failure, the UPS is switched off. Run on battery mode is indicated by the orange LED and the UPS regularly beeps. If the batteries are discharged the UPS switches the outputs off and goes into standby on battery mode. In this mode the UPS stays for one minute, then switches itself off.

Then user can switch the UPS by pushing the ON/OFF button for more than four seconds, during this time the UPS constantly beeps.

### 7.3.2 Battery Operation

If the mains line is not available, the UPS goes directly into run-on-battery mode after the ON/OFF button is pressed for less than four seconds and released. The bypass is not available during battery operation. The UPS can be switched off by the user in the same way as in on-line operation. If the mains line is restored during battery operation, the UPS goes automatically into the run on-line mode.
7.3.3 Remote Operation

If the UPS is connected to the PC it can be controlled by the FreeMaster software. The FreeMaster's control page offers the same interface, so that the UPS can be controlled from in the same way. The remote control works in parallel with the user interface.

Figure 7-6. UPS Project in FreeMaster

In addition to remote control, the FreeMaster displays the values of some variables. There is also a recorder and scope showing the output voltage and temperature of the power stage.
Appendix A. Schematics

A.1 Schematics of Power Stage
Figure 7-7. Block Schematic
Figure 7-8. Auxiliary Power Supplies
Figure 7-9. Battery Charger
Figure 7-10. Control Board Interface
Figure 7-11. dc/dc Step-Up Converter
Figure 7-12. Analog Sensing Circuits
Figure 7-13. PFC and Inverter IGBT Drivers
Figure 7-14. PFC and Inverter
Figure 7-15. PFC Current Control Circuit
A.2 Schematics of User Interface
A.3 Schematics of Input Filter
## A.4 Parts List of UPS Power Stage

### Table A-1. Parts List of UPS Power Stage (Sheet 1 of 5)

<table>
<thead>
<tr>
<th>Reference</th>
<th>Qty</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part number</th>
</tr>
</thead>
<tbody>
<tr>
<td>CT1</td>
<td>1</td>
<td>current transformer — custom design</td>
<td>TRONIC</td>
<td>3044202</td>
</tr>
<tr>
<td>CT2</td>
<td>1</td>
<td>current transformer</td>
<td>COILCRAFT</td>
<td>CS2106</td>
</tr>
<tr>
<td>C200, C209, C221, C303, C308, C610, C611, C632, C633</td>
<td>9</td>
<td>100-nF ceramic SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C201, C205, C208, C211, C212, C213</td>
<td>6</td>
<td>100-pF ceramic SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C202, C203, C207, C210, C214</td>
<td>5</td>
<td>100-µF/16-V radial electrolytic 5 x 11 mm</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C204</td>
<td>1</td>
<td>47-nF ceramic SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C206</td>
<td>1</td>
<td>330-µF/35-V radial electrolytic 10 x 20 mm</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C215, C217</td>
<td>2</td>
<td>220-µF/35-V radial electrolytic 10 x 20 mm</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C216, C218</td>
<td>2</td>
<td>22-µF/50-V 5 x 11 mm</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C219, C220</td>
<td>2</td>
<td>22-µF/20-V tantalum size D</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C300</td>
<td>1</td>
<td>220n ceramic SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C301</td>
<td>1</td>
<td>4.7-nF polyester</td>
<td>Vishay</td>
<td>MKT1820</td>
</tr>
<tr>
<td>C302</td>
<td>1</td>
<td>220-µF/450-V electrolytic</td>
<td>EPCOS</td>
<td>B43504</td>
</tr>
<tr>
<td>C304, C305</td>
<td>2</td>
<td>220-µF/50-V electrolytic</td>
<td>Rubycon</td>
<td>ZL series</td>
</tr>
<tr>
<td>C306</td>
<td>1</td>
<td>100-µF/50-V electrolytic</td>
<td>Jamicon</td>
<td></td>
</tr>
<tr>
<td>C307</td>
<td>1</td>
<td>47-µF/10-V electrolytic</td>
<td>Jamicon</td>
<td></td>
</tr>
<tr>
<td>C309, C310, C311</td>
<td>3</td>
<td>470-nF ceramic SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C312</td>
<td>1</td>
<td>10-nF/100-V ceramic</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C313</td>
<td>1</td>
<td>100-nF/100-V ceramic</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R208, C314, C630, R665, R666, R673, R674, R675</td>
<td>8</td>
<td>no populated</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C315, C316, C600, C613, C616, C623, C624, C626, C627, C628, C634</td>
<td>11</td>
<td>100n ceramic SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C500, C511</td>
<td>2</td>
<td>100n ceramic SMD 1206</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C501, C506</td>
<td>2</td>
<td>22n/400-V metallized</td>
<td>WIMA</td>
<td>MKP10</td>
</tr>
<tr>
<td>C502, C503, C504, C505, C512, C513</td>
<td>6</td>
<td>680µ/50-V</td>
<td>Rubycon</td>
<td>ZL series</td>
</tr>
<tr>
<td>C507, C508</td>
<td>2</td>
<td>1n/100-V</td>
<td>WIMA</td>
<td>MKS2</td>
</tr>
<tr>
<td>C509, C510</td>
<td>2</td>
<td>47-µF/25-V radial electrolytic 5 x 11 mm</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C601</td>
<td>1</td>
<td>10-µ/15-V tantalum size D</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C602, C608</td>
<td>2</td>
<td>330-µF/450-V electrolytic</td>
<td>EPCOS</td>
<td>B43504</td>
</tr>
<tr>
<td>C603, C607</td>
<td>2</td>
<td>22-nF/630-Vdc</td>
<td>WIMA</td>
<td>MKP 10</td>
</tr>
<tr>
<td>C604, C606</td>
<td>2</td>
<td>4.7-nF/Y1</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C605</td>
<td>1</td>
<td>3.3-µF/400-V</td>
<td>WIMA</td>
<td>MKP10</td>
</tr>
<tr>
<td>C609</td>
<td>1</td>
<td>100-nF ceramic SMD 1206</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C612, C629, C631</td>
<td>3</td>
<td>10n ceramic SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C614</td>
<td>1</td>
<td>22-µF/16-V radial electrolytic 5 x 11 mm</td>
<td>any available</td>
<td></td>
</tr>
</tbody>
</table>
### Table A-1. Parts List of UPS Power Stage (Sheet 2 of 5)

<table>
<thead>
<tr>
<th>Reference</th>
<th>Qty</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part number</th>
</tr>
</thead>
<tbody>
<tr>
<td>C617, C620, C622, C625</td>
<td>4</td>
<td>33n ceramic SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C619</td>
<td>1</td>
<td>10-µF/25-V radial electrolytic 5 x 11 mm</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>C621</td>
<td>1</td>
<td>15n ceramic SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>D201,D205,D208, D304</td>
<td>4</td>
<td>LL4448 signal diode</td>
<td>Fairchild</td>
<td>LL4448</td>
</tr>
<tr>
<td>D202,D206,D209</td>
<td>3</td>
<td>zener diode 15-V</td>
<td>Philips</td>
<td>BZV55/15V</td>
</tr>
<tr>
<td>D203,D207,D616,D617</td>
<td>4</td>
<td>zener diode 5.1-V</td>
<td>Philips</td>
<td>BZV55/5V1</td>
</tr>
<tr>
<td>D204</td>
<td>1</td>
<td>high-speed switching diode</td>
<td>ON Semiconductor</td>
<td>MMBD914LT1</td>
</tr>
<tr>
<td>D210,D213</td>
<td>2</td>
<td>schottky diode</td>
<td>ON Semiconductor</td>
<td>MBRA140</td>
</tr>
<tr>
<td>D211,D214</td>
<td>2</td>
<td>LED diode SMD green</td>
<td>Kingbright</td>
<td>KA3528SGT</td>
</tr>
<tr>
<td>D300</td>
<td>1</td>
<td>high-speed diode</td>
<td>Philips</td>
<td>1N4148</td>
</tr>
<tr>
<td>D301</td>
<td>1</td>
<td>ultra fast diode</td>
<td>Vishay</td>
<td>BYW29E-200</td>
</tr>
<tr>
<td>D302</td>
<td>1</td>
<td>bridge rectifier</td>
<td>Diotec Semiconductor</td>
<td>B250R</td>
</tr>
<tr>
<td>D303</td>
<td>1</td>
<td>transient voltage suppressor</td>
<td>Vishay</td>
<td>P6KE200</td>
</tr>
<tr>
<td>D305</td>
<td>1</td>
<td>ultra fast diode</td>
<td>Vishay</td>
<td>BYV26C</td>
</tr>
<tr>
<td>D307,D308</td>
<td>2</td>
<td>general purpose diode</td>
<td>Philips</td>
<td>BAV103</td>
</tr>
<tr>
<td>D309</td>
<td>1</td>
<td>zener diode 5V1</td>
<td>Philips</td>
<td>BZV55/5V1</td>
</tr>
<tr>
<td>D500,D502,D504,D505</td>
<td>4</td>
<td>fast recovery diode</td>
<td>Fairchild</td>
<td>FFPF05U120STU</td>
</tr>
<tr>
<td>D501,D503</td>
<td>2</td>
<td>ultra fast diode</td>
<td>ON Semiconductor</td>
<td>MUR180</td>
</tr>
<tr>
<td>D600</td>
<td>1</td>
<td>diode</td>
<td>Philips</td>
<td>1N4007</td>
</tr>
<tr>
<td>D601</td>
<td>1</td>
<td>schottky diode</td>
<td>ON Semiconductor</td>
<td>MBRS130</td>
</tr>
<tr>
<td>D602,D603,D605,D607,D611,D613,D621,D622,D623</td>
<td>9</td>
<td>schottky diode</td>
<td>Philips</td>
<td>BAT42</td>
</tr>
<tr>
<td>D604,D608</td>
<td>2</td>
<td>hyperfast diode</td>
<td>Fairchild</td>
<td>RHRP8120</td>
</tr>
<tr>
<td>D606</td>
<td>1</td>
<td>bridge rectifier</td>
<td>Diotec Semiconductor</td>
<td>KBPC606</td>
</tr>
<tr>
<td>D609,D610,D612,D614,D615,D618,D619</td>
<td>7</td>
<td>schottky diode</td>
<td>ON Semiconductor</td>
<td>MBR0540</td>
</tr>
<tr>
<td>D620</td>
<td>1</td>
<td>zener diode 3V6</td>
<td>Philips</td>
<td>BZV55/3V6</td>
</tr>
<tr>
<td>D624,D626,D628</td>
<td>3</td>
<td>zener diode 15 V</td>
<td>Philips</td>
<td>BZV55/15V</td>
</tr>
<tr>
<td>D625,D627</td>
<td>2</td>
<td>zener diode 5.1 V</td>
<td>Philips</td>
<td>BZV55/5V1</td>
</tr>
<tr>
<td>F100</td>
<td>1</td>
<td>fast fuse 2 A</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>F101</td>
<td>1</td>
<td>car fuse 40 A</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>F102</td>
<td>1</td>
<td>fast fuse 6.3 A</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>ISO300</td>
<td>1</td>
<td>optocoupler</td>
<td>Vishay</td>
<td>SFH615A-2</td>
</tr>
<tr>
<td>J100,J102,J103,J104,J105,J106,J107,J108,J109</td>
<td>9</td>
<td>FASTON</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J101,J110,J111</td>
<td>3</td>
<td>connector</td>
<td>EZK (distributor)</td>
<td>PSH02_02P</td>
</tr>
<tr>
<td>J400</td>
<td>1</td>
<td>header 7 x 2</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>J401</td>
<td>1</td>
<td>connector</td>
<td>EZK (distributor)</td>
<td>PFL_20X2</td>
</tr>
<tr>
<td>J402</td>
<td>1</td>
<td>header 5 x 2</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>J403</td>
<td>1</td>
<td>header 13 x 2</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>L200,L205</td>
<td>2</td>
<td>220-µH axial inductor 130 mA</td>
<td>FASTRON</td>
<td></td>
</tr>
<tr>
<td>Reference</td>
<td>Qty</td>
<td>Description</td>
<td>Manufacturer</td>
<td>Part number</td>
</tr>
<tr>
<td>-----------</td>
<td>-----</td>
<td>-------------</td>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>L201, L500, L503, L504</td>
<td>4</td>
<td>330µ radial inductor 500 mA</td>
<td>FASTRON</td>
<td></td>
</tr>
<tr>
<td>L202</td>
<td>1</td>
<td>470 µH</td>
<td>FASTRON</td>
<td>09P/F-471k</td>
</tr>
<tr>
<td>L203</td>
<td>1</td>
<td>680 µH</td>
<td>FASTRON</td>
<td>09P/F-681k</td>
</tr>
<tr>
<td>L204</td>
<td>1</td>
<td>1-µ axial inductor 1.2 A</td>
<td>FASTRON</td>
<td></td>
</tr>
<tr>
<td>L300, L301</td>
<td>2</td>
<td>radial inductor 47 µH</td>
<td>Coilcraft</td>
<td>PCV-1-473-03</td>
</tr>
<tr>
<td>L501, L502</td>
<td>2</td>
<td>560µ / 1 A</td>
<td>Coilcraft</td>
<td>PCV-2-564-02</td>
</tr>
<tr>
<td>L505</td>
<td>1</td>
<td>2.5 mH</td>
<td>custom design</td>
<td>see 4.5.2.1</td>
</tr>
<tr>
<td>L506</td>
<td>1</td>
<td>5 mH</td>
<td>custom design</td>
<td>see 4.5.4.2</td>
</tr>
<tr>
<td>L507</td>
<td>1</td>
<td>toroid choke</td>
<td>Tesla Blatna</td>
<td>TL34P</td>
</tr>
<tr>
<td>Q200, Q602, Q603, Q604, Q607</td>
<td>5</td>
<td>general-purpose bipolar transistor</td>
<td>ON Semiconductor</td>
<td>BC846</td>
</tr>
<tr>
<td>Q201, Q601</td>
<td>2</td>
<td>Power MOSFET transistor</td>
<td>ON Semiconductor</td>
<td>NTF3055</td>
</tr>
<tr>
<td>Q300</td>
<td>1</td>
<td>general-purpose bipolar transistor</td>
<td>ON Semiconductor</td>
<td>BC847</td>
</tr>
<tr>
<td>Q301, Q302, Q609, Q610</td>
<td>4</td>
<td>Power MOSFET transistor</td>
<td>ON Semiconductor</td>
<td>MMBF0201NLT1</td>
</tr>
<tr>
<td>Q500, Q501, Q502, Q503</td>
<td>4</td>
<td>Power MOSFET transistor</td>
<td>ON Semiconductor</td>
<td>NTP45N06</td>
</tr>
<tr>
<td>Q600</td>
<td>1</td>
<td>temperature sensor</td>
<td>National Semiconductor</td>
<td>LM35CA</td>
</tr>
<tr>
<td>Q605, Q608</td>
<td>2</td>
<td>IGBT</td>
<td>Fairchild</td>
<td>HGTG10N120BND</td>
</tr>
<tr>
<td>Q606</td>
<td>1</td>
<td>IGBT</td>
<td>International Rectifier</td>
<td>IRG4IBC20W</td>
</tr>
<tr>
<td>Q611, Q612</td>
<td>2</td>
<td>no populated</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RE1, RE2, RE3</td>
<td>3</td>
<td>relay</td>
<td>CARLO GAVAZZI</td>
<td>MZPA001</td>
</tr>
<tr>
<td>RE4</td>
<td>1</td>
<td>relay</td>
<td>CARLO GAVAZZI</td>
<td>MZPA002</td>
</tr>
<tr>
<td>R200, R203</td>
<td>2</td>
<td>510 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R201, R204, R205, R211, R316, R322</td>
<td>6</td>
<td>220 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R202</td>
<td>1</td>
<td>15k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R206</td>
<td>1</td>
<td>16k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R207, R657, R680</td>
<td>3</td>
<td>33 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R209, R323, R324, R329, R623, R632, R645, R652</td>
<td>8</td>
<td>1k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R210</td>
<td>1</td>
<td>1.8 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R212, R317, R325</td>
<td>3</td>
<td>33k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R213, R314, R331, R663, R668</td>
<td>5</td>
<td>100 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R214</td>
<td>1</td>
<td>2.4k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R215</td>
<td>1</td>
<td>20k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R216</td>
<td>1</td>
<td>1.8k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R300</td>
<td>1</td>
<td>precision shunt resistor</td>
<td>Isabellenhütte Heusler GmbH KG</td>
<td>PMA-C - R100 - 1</td>
</tr>
<tr>
<td>R301</td>
<td>1</td>
<td>68k, 2W</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R302, R306</td>
<td>2</td>
<td>1M size 0207</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R303</td>
<td>1</td>
<td>24k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R304</td>
<td>1</td>
<td>39k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R305</td>
<td>1</td>
<td>1k8 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R307</td>
<td>1</td>
<td>620 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R308</td>
<td>1</td>
<td>3K6 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>Reference</td>
<td>Qty</td>
<td>Description</td>
<td>Manufacturer</td>
<td>Part number</td>
</tr>
<tr>
<td>-----------</td>
<td>-----</td>
<td>-------------</td>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>R309</td>
<td>1</td>
<td>2k4 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R310</td>
<td>1</td>
<td>5k6 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R311, R636</td>
<td>2</td>
<td>33k, size 0207</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R312</td>
<td>1</td>
<td>200 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R313</td>
<td>1</td>
<td>27R SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R315</td>
<td>1</td>
<td>7.5k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R318, R320, R615, R617</td>
<td>4</td>
<td>100k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R319, R321</td>
<td>2</td>
<td>1k6 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R326</td>
<td>1</td>
<td>3k9 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R327</td>
<td>1</td>
<td>560 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R328</td>
<td>1</td>
<td>68k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R330, R508, R509, R640, R641, R642, R644, R645, R655, R656, R658, R659, R660, R669, R670</td>
<td>15</td>
<td>10k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R500, R505, R506, R507, R606</td>
<td>5</td>
<td>10 SMD 1206</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R501, R502</td>
<td>2</td>
<td>1-k/5-W</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R503, R504</td>
<td>2</td>
<td>100R/1W</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R600</td>
<td>1</td>
<td>10 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R601</td>
<td>1</td>
<td>68 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R602, R603, R604, R605</td>
<td>4</td>
<td>4K7 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R607, R610, R613</td>
<td>3</td>
<td>100 SMD 1206</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R608, R611</td>
<td>2</td>
<td>330 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R609, R612</td>
<td>2</td>
<td>33 SMD 1206</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R614</td>
<td>1</td>
<td>130RSMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R616, R678, R679</td>
<td>3</td>
<td>180 SMD 1206</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R618, R626, R627, R628, R643, R646, R647, R648</td>
<td>8</td>
<td>330k size 0207</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R619, R625, R629, R630, R634, R635, R638, R639</td>
<td>8</td>
<td>300k size 0207</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R620, R621, R633, R649, R672</td>
<td>5</td>
<td>11k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R622</td>
<td>1</td>
<td>470k size 0207</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R624, R667</td>
<td>2</td>
<td>0R SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R631</td>
<td>1</td>
<td>130k size 0207</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R637, R651</td>
<td>2</td>
<td>680k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R650, R653</td>
<td>2</td>
<td>10k SMD 4315</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R661, R662</td>
<td>2</td>
<td>470 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R664</td>
<td>1</td>
<td>1.6k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R671</td>
<td>1</td>
<td>4.7k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>T1</td>
<td>1</td>
<td>transformer</td>
<td>customer design</td>
<td>see 4.3.1</td>
</tr>
<tr>
<td>T300</td>
<td>1</td>
<td>transformer</td>
<td>customer design</td>
<td>see 4.2.4</td>
</tr>
<tr>
<td>T500</td>
<td>1</td>
<td>transformer</td>
<td>customer design</td>
<td>see 4.4.2.1</td>
</tr>
<tr>
<td>U200</td>
<td>1</td>
<td>switching regulator</td>
<td>ON Semiconductor</td>
<td>LM2575-ADJ</td>
</tr>
<tr>
<td>U201</td>
<td>1</td>
<td>switching regulator</td>
<td>ON Semiconductor</td>
<td>UC3843</td>
</tr>
<tr>
<td>U202</td>
<td>1</td>
<td>switching regulator</td>
<td>ON Semiconductor</td>
<td>LM2575-5</td>
</tr>
</tbody>
</table>
## Table A-1. Parts List of UPS Power Stage (Sheet 5 of 5)

<table>
<thead>
<tr>
<th>Reference</th>
<th>Qty</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part number</th>
</tr>
</thead>
<tbody>
<tr>
<td>U203</td>
<td>1</td>
<td>linear regulator</td>
<td>ON Semiconductor</td>
<td>MC78L05ACP</td>
</tr>
<tr>
<td>U300</td>
<td>1</td>
<td>switching regulator</td>
<td>Power Integrations</td>
<td>TOP249Y</td>
</tr>
<tr>
<td>U301, U604</td>
<td>1</td>
<td>operational amplifier</td>
<td>ON Semiconductor</td>
<td>MC33502</td>
</tr>
<tr>
<td>U302</td>
<td>1</td>
<td>voltage reference</td>
<td>Fairchild</td>
<td>TL431ACD</td>
</tr>
<tr>
<td>U500, U501</td>
<td>2</td>
<td>MOSFET driver</td>
<td>ON Semiconductor</td>
<td>MC33152D</td>
</tr>
<tr>
<td>U601</td>
<td>1</td>
<td>opto driver</td>
<td>Agilent</td>
<td>HCPL3150</td>
</tr>
<tr>
<td>U605</td>
<td>1</td>
<td>dual comparators</td>
<td>ON Semiconductor</td>
<td>LM393D</td>
</tr>
<tr>
<td>U606</td>
<td>1</td>
<td>quad comparators</td>
<td>ON Semiconductor</td>
<td>LM339M</td>
</tr>
<tr>
<td>U615</td>
<td>1</td>
<td>opto driver</td>
<td>Agilent</td>
<td>HCPL-315J</td>
</tr>
</tbody>
</table>

## A.5 Parts List of User Interface

## Table A-2. Parts List of User Interface

<table>
<thead>
<tr>
<th>Reference</th>
<th>Qty</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part number</th>
</tr>
</thead>
<tbody>
<tr>
<td>BZ1</td>
<td>1</td>
<td>buzzer</td>
<td>EZK (distributor)</td>
<td>SA003</td>
</tr>
<tr>
<td>D1, D10</td>
<td>3</td>
<td>LED diode red</td>
<td>Kingbright</td>
<td>L53LID</td>
</tr>
<tr>
<td>D2, D5, D6, D7, D8, D9</td>
<td>6</td>
<td>LED diode green</td>
<td>Kingbright</td>
<td>L53LGD</td>
</tr>
<tr>
<td>D3</td>
<td>1</td>
<td>LED diode orange</td>
<td>Kingbright</td>
<td>L53ND</td>
</tr>
<tr>
<td>D4</td>
<td>1</td>
<td>LED diode yellow</td>
<td>Kingbright</td>
<td>L53LYD</td>
</tr>
<tr>
<td>J1</td>
<td>1</td>
<td>header 13 x 2</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>J2, J5</td>
<td>2</td>
<td>connector CANNON 9 pin</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>J3, J6</td>
<td>2</td>
<td>header 5 x 2</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>J4</td>
<td>1</td>
<td>connector</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R1, R3, R6, R7, R8, R9, R10, R11, R12</td>
<td>9</td>
<td>1300 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R2, R4</td>
<td>2</td>
<td>10k SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>R5</td>
<td>1</td>
<td>270 SMD 0805</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>SW1</td>
<td>1</td>
<td>Switch</td>
<td>MEC</td>
<td>switch 15501</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>extender 16250</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>cap 1D06</td>
</tr>
<tr>
<td>SW2</td>
<td>1</td>
<td>Switch</td>
<td>MEC</td>
<td>switch 15501</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>extender 16250</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>cap 1D02</td>
</tr>
</tbody>
</table>
A.6 Parts List of Input Filter

Table A-3. Parts List of Input Filter

<table>
<thead>
<tr>
<th>Reference</th>
<th>Qty</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part number</th>
</tr>
</thead>
<tbody>
<tr>
<td>C100B</td>
<td>1</td>
<td>1−µF / X1</td>
<td>EPCOS</td>
<td>B81133</td>
</tr>
<tr>
<td>C100, C101</td>
<td>2</td>
<td>100-nF / X1</td>
<td>EPCOS</td>
<td>B81133</td>
</tr>
<tr>
<td>C102, C103</td>
<td>2</td>
<td>4.7-nF / Y1</td>
<td>MURATA</td>
<td>DE2E3KH472MA3B</td>
</tr>
<tr>
<td>J100,J101,J102,J103,J104</td>
<td>5</td>
<td>faston 6.3 mm</td>
<td>any available</td>
<td></td>
</tr>
<tr>
<td>L100</td>
<td>1</td>
<td>toroid choke</td>
<td>Tesla Blatna</td>
<td>TL34P</td>
</tr>
<tr>
<td>R100</td>
<td>1</td>
<td>inrush current limiter</td>
<td>Rhopoint Components</td>
<td>SG-190</td>
</tr>
<tr>
<td>R101, R102</td>
<td>2</td>
<td></td>
<td>EPCOS</td>
<td>SIOV-S20K275</td>
</tr>
<tr>
<td>R103</td>
<td>1</td>
<td>330k, 0.6 W</td>
<td>any available</td>
<td></td>
</tr>
</tbody>
</table>
Appendix B. References


5. International Standard IEC62040-1-1, Uninterruptable power systems (UPS) - Part 1-2: General and safety requirements for UPS used in operator access areas.


10. TOP242-250 Up to 290 W Extended power, design flexible, EcoSmart, integrated off-line switcher family, data sheet. Power Integrations, August 2003


33. MC9S12E128 Controller Board, Design Reference Manual, Motorola 2004

Single Phase On-Line UPS Using MC9S12E128
### Appendix C. Glossary

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>ac</td>
<td>alternating current</td>
</tr>
<tr>
<td>ac/dc converter</td>
<td>a converter that converts alternating voltage (ac) to direct voltage (dc)</td>
</tr>
<tr>
<td>ATD</td>
<td>analog-to-digital converter</td>
</tr>
<tr>
<td>A/D</td>
<td>analog-to-digital</td>
</tr>
<tr>
<td>AVR</td>
<td>automatic voltage regulation</td>
</tr>
<tr>
<td>CW</td>
<td>CodeWarrior; compilers produced by Metrowerks</td>
</tr>
<tr>
<td>DAC</td>
<td>digital-to-analog converter</td>
</tr>
<tr>
<td>dc</td>
<td>direct current</td>
</tr>
<tr>
<td>dc/ac converter</td>
<td>a converter that converts direct voltage (dc) to alternating voltage (ac)</td>
</tr>
<tr>
<td>dc/dc converter</td>
<td>converter that converts one level of direct voltage to another level of direct voltage</td>
</tr>
<tr>
<td>DT</td>
<td>dead time; a short time that must be inserted between turning off one transistor in the inverter half-bridge and turning on the complementary transistor, to allow for the limited switching speed of the transistors.</td>
</tr>
<tr>
<td>duty cycle</td>
<td>the ratio of the time the signal is on to the time it is off. Duty cycle is usually quoted as a percentage.</td>
</tr>
<tr>
<td>EMC</td>
<td>electro magnetic compatibility</td>
</tr>
<tr>
<td>EMI</td>
<td>electro magnetic interference</td>
</tr>
<tr>
<td>IC</td>
<td>integrated circuit</td>
</tr>
<tr>
<td>IDE</td>
<td>integrated development environment</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated gate bipolar transistor</td>
</tr>
<tr>
<td>input/output (I/O)</td>
<td>input/output interfaces between a computer system and the external world. A CPU reads an input to sense the level of an external signal and writes to an output to change the level on an external signal.</td>
</tr>
<tr>
<td>interrupt</td>
<td>a temporary break in the sequential execution of a program to respond to signals from peripheral devices by executing a subroutine.</td>
</tr>
<tr>
<td>logic 1</td>
<td>a voltage level approximately equal to the input power voltage ($V_{DD}$)</td>
</tr>
<tr>
<td>logic 0</td>
<td>a voltage level approximately equal to the ground voltage ($V_{SS}$)</td>
</tr>
<tr>
<td>HCS12</td>
<td>a Freescale Semiconductor family of 16-bit MCUs</td>
</tr>
</tbody>
</table>
| MCU                | microcontroller unit; a complete computer system, including a CPU, memory, a clock oscillator, and input/output (I/O) on a single integrated circuit
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MW</td>
<td>Metrowerks Corporation</td>
</tr>
<tr>
<td>PC</td>
<td>personal computer</td>
</tr>
<tr>
<td>PCB</td>
<td>printed circuit board</td>
</tr>
<tr>
<td>PCM</td>
<td>PC master software for communication between PC and system</td>
</tr>
<tr>
<td>PFC</td>
<td>power factor correction</td>
</tr>
<tr>
<td>PI Controller</td>
<td>proportional-integral controller</td>
</tr>
<tr>
<td>PID Controller</td>
<td>proportional-integral-derivative controller</td>
</tr>
<tr>
<td>PLL</td>
<td>phase-locked loop; a clock generator circuit in which a voltage controlled oscillator produces an oscillation that is synchronized to a reference signal</td>
</tr>
<tr>
<td>PMP</td>
<td>FreeMaster software project file</td>
</tr>
<tr>
<td>PVAL</td>
<td>PWM value register of motor control PWM module of the MC9S12E128 microcontroller; it defines the duty cycle of the generated PWM signal.</td>
</tr>
<tr>
<td>PWM</td>
<td>pulse width modulation</td>
</tr>
<tr>
<td>RESET</td>
<td>to force a device to a known condition</td>
</tr>
<tr>
<td>RMS</td>
<td>root mean square</td>
</tr>
<tr>
<td>SCI</td>
<td>serial communications interface module; a module that supports asynchronous communication</td>
</tr>
<tr>
<td>SMPS</td>
<td>switched mode power supply</td>
</tr>
<tr>
<td>software</td>
<td>instructions and data that control the operation of a microcontroller</td>
</tr>
<tr>
<td>SPI</td>
<td>serial peripheral interface module; a module that supports synchronous communication</td>
</tr>
<tr>
<td>SWI</td>
<td>software interrupt; an instruction that causes an interrupt and its associated vector fetch</td>
</tr>
<tr>
<td>THD</td>
<td>total harmonic distortion</td>
</tr>
<tr>
<td>timer</td>
<td>A module used to relate events in a system to a point in time</td>
</tr>
<tr>
<td>UPS</td>
<td>uninterruptable power supply</td>
</tr>
</tbody>
</table>
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