Fact Sheet

AFD4400
Integrated solution for digital front end processor applications

Overview

The AFD4400 Airfast digital front end (DFE) processor combines the digital components of a cellular base station radio onto a single integrated circuit. Breaking stride with traditional hardwired solutions, the signal processing paths of the AFD4400 execute on an array of vector signal processors. With a combined Vector Signal Processor Accelerator (VSPA) throughput of 1.76 teraflops, the AFD4400 easily supports LTE, W-CDMA, CDMA and GSM networks in single and multi-mode configurations with up to 100 MHz of RF bandwidth in 4 antenna configurations. The flexible, software-based approach allows the device to easily scale from 1 to 8 antennas, while aggressive power management techniques ensure power dissipation dynamically adjusts to changing load conditions.

The AFD4400 uses industry-standard interfaces to connect with other system components, including common public radio interface (CPRI) for modem links, Ethernet for operations and maintenance links, JESD204B for transceiver interfaces and Antenna Interface Standards Group (AISG) for tower-mounted equipment links.

While primarily designed for cellular applications, the AFD4400 is also appropriate for radar, military and commercial broadcast applications.

The block diagram below illustrates the high-level architecture of the DFE processor. Signal processing is partitioned into data processing paths for transmit processing, receive processing and sample processing. An ARM® Cortex®-A9 processor provides local control for the RF subsystem. It is augmented with a hierarchical on- and off-chip memory system linked by a multi-level AXI interconnect fabric. A full complement of support peripherals enables a glueless system in most applications.

AFD4400 Block Diagram—Digital Front End General Features

Target Applications
- Cellular base stations
- Remote radio heads
- Active antennas
- Radar
- Military countermeasures
Reference Hardware and Software and Development Tools

Freescale supports the AFD4400 SoC with a complete reference design ecosystem. Hardware components include a reference design digital board (RDB), a choice of 307 MSPS integrated or 491/983 MSPS discrete transceiver cards, a shielding chassis, and a wide range of PA reference designs spanning the full range of frequency bands and power levels.

The RDB comes with Linux® pre-installed. This Linux port is based on the 3.8.4 kernel including the PREEMPT_RT patch, and has been customized for cellular radio applications. An application programmer interface (API) is defined at multiple levels and promotes code reuse and eases porting of proprietary control plane stacks. Closed-loop, CPRI-to-JESD204 transmit and receive test applications enable out-of-the-box evaluation of AFD4400 performance and provide customers a framework for custom application development.

A vector signal processing library provides developers a jump start into datapath application development. Optimized vector processor assembly functions and MATLAB bit-exact equivalents are supplied for signal processing building blocks such as FIR filters, interpolation/decimation, FFT and IFFT, LLS and RLS, frequency translation and mixing. Application-level reference designs are available for digital up-conversion (DUC), digital down conversion (DDC), crest factor reduction (CFR) and digital pre-distortion (DPD) with closed-loop adaptation.

AFD4400 Features and Benefits

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<th>Key Features</th>
<th>Benefits</th>
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<td>Fully programmable signal processing paths</td>
<td>More flexible than hardwired ASICs. Faster design turnaround and lower power than FPGAs.</td>
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<td>Industry-standard interfaces (CPRI, JESD204B, AISG, Ethernet)</td>
<td>Easily integrates with existing system components.</td>
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<td>Vector signal processor function library and application reference designs</td>
<td>Enable fast application development for quicker time to market.</td>
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<td>Linux board support package with radio control APIs</td>
<td>No-cost, royalty-free software base to build your radio control plane software</td>
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<td>Flexible clocking and synchronization architecture</td>
<td>Supports recovery of frequency-corrected clock from CPRI link. Mechanisms provided for multi-device synchronization required in large antenna arrays.</td>
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<td>Aggressive power management techniques</td>
<td>Power consumption scales with application load for tomorrow’s power-conscious networks</td>
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<td>Application reference designs optimized for Freescale power amplifiers</td>
<td>Obtaining the highest efficiency and linearity is key to any radio design. Freescale has done the hard part for you with jointly optimized reference designs and DPD algorithms.</td>
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CodeWarrior Tool Suite Accelerates Multi-Core VSPA Software Development

CodeWarrior Development Studio for VSPA provides a complete Eclipse-based development environment, including an optimizing compiler, assembler and linker. A cycle-accurate simulator and performance analysis tools enable pre-hardware development, while the multi-core enabled debugger, trace and analysis tools aid on-silicon debugging. The open-source Eclipse framework allows easy extension and customization.

For more information, visit freescale.com/RF