Instrument Cluster Design Based on the Latest 32-bit MCU Featuring Basic and Advanced Graphic Capabilities

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Agenda

• Introduction and Overview
• Cores and Platform
• External Memory
• Graphics Capabilities
• Safety and Security
• Software
• Summary
Consumers Driving Demand for Vivid Cutting-Edge Instrument Cluster Graphics

• Automotive instrument cluster manufacturers continue to see increasing consumer demand for cutting-edge quality graphics
• Demand for larger single or dual high-resolution graphics displays with mechanical gauges drive a bulk of the market moving forward

• Attach rates for heads-up display projected to increase, significantly keeping pace with requirements for increased driver awareness
Automotive Instrument Cluster Manufacturer Market Trends

- OEMs, and their suppliers, are projected to invest in platform solutions with low-cost expansion capabilities allowing them to easily adapt to regional or increasing customer requirements.
- ARM®-based architecture is growing in popularity.
- Integrated safety and security is a growing requirement with today’s cyber-security concerns.
- High performance graphics are desired but with low memory footprints and simplified development environments.
Industry’s highest performance, single-chip MCUs enabling the next generation of automotive instrument cluster graphics design

Industry’s highest performance, triple-core, single-chip instrument cluster solution based on ARM® technology combining an ARM Cortex-M4 core (for real-time vehicle processing) and an ARM Cortex-A5 core (for high-quality graphics) with a ARM Cortex-M0+ core (as an I/O processor to autonomously control stepper motors).

Superior capability and quality graphics with low memory and CPU overhead achieved through differentiating graphics hardware which enables the highly efficient use of on-chip memory

Scalable solution is easily optimized to specific requirements enabling global platforms that can be easily optimized for regional requirements
Driver Information Systems Roadmap

**Applications**

- **High-end**
  - Best Graphics, Performance & Integration
- **Mid-range**
  - Optimized Graphics, High Integration
  - Cost Effective Performance
- **Low-end**
  - Lowest System Cost, High Integration

**Color Graphics**

- **1st Si**
  - Proposal
  - Planning
  - Execution
  - Production

**2011 - 2016**

- **High-end**
  - **May 12**
    - I.MX 6 DUAL
      - ARM Cortex-Dual A7/M4, VSPA, 2D-ACE, GC355
  - **Jan 12**
    - I.MX53
  - **Jun 14**
    - MAC57D5xx
      - ARM Cortex-A5/M4/M0+, 2D-ACE, 2D-GPU, GC355

- **Mid-range**
  - **Jan 13**
    - SVF5/3R (Vybrid)
  - **Aug 12**
    - I.MX 6 DUALITE
      - ARM Cortex-Dual A7/M4, VSPA, 2D-ACE, GC355

- **Low-end**
  - **Nov 12**
    - S12ZVHY (Lumen-2W)
  - **May 13**
    - I.MX 6 SOLO
  - **Jun 14**
    - I.MX53
  - **Aug 12**
    - S12ZH (Lumen-4WL)

**Power Architecture**

- **ARM Cortex-Dual A5/M4, 2D-ACE, GC355**
- **ARM Cortex-A5/M4/M0+, 2D-ACE, 2D-GPU, GC355**
- **ARM Cortex-Dual A7/M4, VSPA, 2D-ACE, GC355**

**Freescale**

Reflects Lead Customer Timing
Introducing: MAC57D5xx - Block Diagram

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<th>Power Management</th>
<th>ARM® Cortex™-A5</th>
<th>ARM® Cortex™-M4</th>
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<tr>
<td>Single 3.3V supply</td>
<td>Up to 320 MHz</td>
<td>Up to 160 MHz</td>
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<tr>
<td>Low Voltage Detection</td>
<td>NEON / FPU / MMU</td>
<td>FPU</td>
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<tr>
<td>Low Power Control</td>
<td>32K / 32K L1 cache</td>
<td>16K / 16K L1 cache</td>
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<thead>
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<th>System and General Purpose</th>
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<tr>
<td>Memory Protection</td>
<td>DMA</td>
<td>I/O Processor</td>
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<tr>
<td>Security - CSE2</td>
<td>Autonomous RTC</td>
<td>ARM® Cortex™-M0+</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Up to 80 MHz</td>
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<tr>
<td></td>
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<td>32K ECC SRAM</td>
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<thead>
<tr>
<th>Peripherals</th>
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<tr>
<td>CAN(FD) x3</td>
<td>I²C x2</td>
<td>I/O Processor (ARM Cortex M0+)</td>
</tr>
<tr>
<td>UART/LIN x3</td>
<td>Watchdog Timers</td>
<td>Supports autonomous operation</td>
</tr>
<tr>
<td>SPI x5</td>
<td>IC/OC Timers / PWM</td>
<td>Stepper Motor Drivers</td>
</tr>
<tr>
<td>MLB 3-wire</td>
<td>SMD / SSD x6</td>
<td>Peripheral control and Low power operation</td>
</tr>
<tr>
<td>10/100 Ethernet + AVB</td>
<td>12-bit SAR ADC</td>
<td></td>
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<tr>
<th>Audio / GFx / Video / Display</th>
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<tbody>
<tr>
<td>SGM (includes I2S)</td>
<td>2D-ACE + inline HUD Warping</td>
<td>Security (CSE2)</td>
</tr>
<tr>
<td>Digital Video In</td>
<td>2D - ACE</td>
<td>Meets SHE specification</td>
</tr>
<tr>
<td>GC355 OpenVG GPU</td>
<td>Open LDI &amp; RSDS</td>
<td>Meets GM’s Global B Cybersecurity requirements</td>
</tr>
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<thead>
<tr>
<th>External Memory</th>
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<tbody>
<tr>
<td>DDR QuadSPI Flash x2</td>
<td>16/32-bit DDR2</td>
<td>Functional Safety</td>
</tr>
<tr>
<td>16-bit SDR</td>
<td></td>
<td>- Built in support for ASIL-B</td>
</tr>
</tbody>
</table>

**ARM® Core Architecture:**
- ARM® Cortex™-M4 vehicle processor
- ARM® Cortex™-A5 application processor
- ARM® Cortex™-M0+ I/O processor

- 4 MByte ECC flash
- 2x 512 KB ECC SRAM
- 1.3 MB non-ECC SRAM

**Supports 2 x WVGA displays:**
- OpenVG 1.1 GPU
- 2 x 2D-ACE display interfaces
  - DigitalRGB, RSDS, LVDS i/f
- Hardware HUD warping engine
- Digital camera input

**Extensive connectivity:**
- Ethernet AVB, MLB50, CAN-FD

**I/O Processor (ARM Cortex M0+)**
- Supports autonomous operation
- Stepper Motor Drivers
- Peripheral control and Low power operation

**Security (CSE2)**
- Meets SHE specification
- Meets GM’s Global B Cybersecurity requirements

**Functional Safety**
- Built in support for ASIL-B

**Software Support**
- AutoSAR
- GC355
- I/OP Stepper motor driver

**BGA and QFP package options:**
- 176/208LQFP + 516MAPBGA
- -40 to +105°C T_A
MAC57D5xx - Product Family Scalability

**Target Applications**
- Instrument clusters
- Heads-up displays
- Multifunction displays

**Standard**
- Cluster with high res. TFT

**Advanced**
- Cluster with dual high res. TFTs

**Premium**
- Cluster with high res. TFT & HUD

**WVGA with only internal memory**
- dRGB & RSDS display interface
- QFP Pin compatible family

**Advanced Communications:**
- Ethernet-AVB / MLB
- SDR DRAM expansion on 2-layer PCB
- Dual display drive and Video input

**DDR2 DRAM expansion**
- On-the-fly hardware HUD warping engine
- OpenLDI LVDS display interface
Platform and Cores
MAC57D5xx Architecture

**Real-Time Domain (CortexM4):**
Prioritises latency over throughput
Predominantly AHB based
Runs AutoSAR / service peripherals

**Application Domain (CortexA5):**
Prioritises throughput over latency
Predominantly AXI based
Runs Graphics application

- **CortexM4 Vehicle Processor**
  - 1.25DMIPS/MHz : 160MHz operation

- **CortexA5 Application Processor**
  - 1.57DMIPS/MHz : 320MHz operation
  - NEON SIMD
  - Memory Management Unit

- **AMBA AXBS & QOS301 Bus interconnect**
  - Mixed AXI/AHB
  - xRDC Memory Protection

- **I/O Processor**
  - CortexM0+
  - Intelligent Stepper Motor Control
  - Low power mode controller

- **Graphics Features**
  - 2 x 2D-ACE display controllers
  - GC355 OpenVG 1.1 GPU
  - GC255 Raster/Vector GPU
  - Digital Video Input
  - 1.3MB Graphics SRAM

- **Shared Embedded Memories**
  - 4MB Embedded Flash
  - 1MB System SRAM

- **Dual DDR QuadSPI Flash expansion**

- **16-bit SDR / 32bit DDR2 DRAM options**
ARM Cortex-A5 Core Features

- **ARM Cortex-A5 processor core**
- **Supports ARMv7-A instruction set architecture**
  - Includes FPU (VFPv3-D16) definition
    - Single & double precision, add, sub, mult, div, mac, sqrt
  - NEON Media Processing Engine (MPE)
    - Extends FPU capability with advanced SIMD instructions for media and signal processing functions over 8, 16, 32-bit integer and 32-bit floating point data types
- **8-stage single issue pipeline implementation operating at 320 MHz**
  - 1.57 DMIPS per MHz integer performance (502 DMIPS @ 320 MHz)
  - 4-stage load/store pipeline
  - 5-stage FPU/MPE pipeline
- **Processor-local Memories**
  - 2 way set-associative 32 Kbyte instruction cache with 32 byte line size
  - 4 way set-associative 32 Kbyte data cache with 32 byte line size
  - Standard CA5 memory management unit
- **64-bit AXI system bus interface supporting multiple outstanding transactions**
ARM Cortex-M4 Processor Core Features

• Supports ARMv7-M instruction set architecture
  - Includes single-precision FPU
    ▪ Single & double precision, add, sub, mult, div, mac, sqrt
• 3-stage single issue pipeline implementation operating at 160 MHz
  - 1.25 DMIPS per MHz integer performance
    (200 DMIPS @ 160 MHz)
• Processor-local memories
  - 2 way set-associative 16 Kbyte code cache with 32 byte line size
  - 2 way set-associative 16 Kbyte system cache with 32 byte line size
    ▪ Write-back and write-through modes of operation
  - 64kB of Tightly Coupled Memory (TCM)
    ▪ Backdoor system bus port provides TCM access to other bus masters
• Memory Protection Unit
• Modified Harvard 64-bit AHB system bus interface + 64-bit AHB backdoor port to TCM
IOP Features

- ARM Cortex CM0+ CPU
- Operates at platform frequency /2, /4, /8, /16....
  - 0.95 DMIPS per MHz (76 DMIPS @ 80 MHz)
- Local 32 kByte SRAM with ECC for code and variables
- Local memory map covering local SRAM and peripherals
- Debug interface with shared access through JTAG/SWO via system DAP

IOP Overview:

- Reduces main CPU workload and interrupt load
- Shared SRAM / registers for motor parameters
- Dedicated 32 kB SRAM
  - Memory mapped for CA5/CM4
  - Serves as system standby RAM
- Enables Intelligent Peripherals:
  - Autonomous stepper motor drive
  - Available to other system peripherals
  - Available in low power ‘IOP’ mode
IOP Peripheral Access / Power Domains

PD2: Performance
(includes core platform, memories)

PD0: Standby

CM0+
8kSRAM RD0
24kSRAM RD1

CM4

CA5

NVIC

GIC

IOP Domain Peripherals:
- ARTC
- LCD
- ACOMPO/1
- WKPU

IOP Interrupt Peripherals:
- DMA0
- MSCM
- PMU
- SMD / SSD
- MC-RGM/ME

IOP Visible Peripherals:
- DMA-CH-mux
- I2C0/1
- FlexTimer1/2/3
- DSPI1-4
- Linflex0-2
- CAN0-2
- CRC

CM4/CA5 Peripherals:
- GC355
- 2D-ACE0/1
- RLE
- TCON
- VIU
- ENET
- ....

Interrupts

Read/Write Access

PD1: IOP

CM4

CA5

NVIC

GIC

IOP Domain

Interrupts

Read/Write Access

Standby Domain Peripherals:
- SWT(CM0+)
- ADC
- FlexTimer0
- PIT
- SIUL2

PD0: Standby

CM0+
8kSRAM RD0
24kSRAM RD1

CM4

CA5

NVIC

GIC

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- VIU
- ENET
- ....

Interrupts

Read/Write Access
Autonomous Real Time Clock

- Real Time Clock with self-wake-up and clock correction logic.
- Autonomous operation in low power modes
- No need to wake full MCU from sleep to calibrate
- Correction Block determines and updates prescaler synchronous to the 1sec tick.
- Correction of 32KHz or internal IRC.
External Memory
QuadSPI Serial Flash Controller

• Dual QuadSPI architecture supports:
  - Two external serial flashes per QuadSPI module
  - SDR and DDR serial flash
  - Programmable Sequence Engine for compatibility to any serial flash
  - Supports XIP: code flash expansion
  - First MCU to support Spansion’s Hyperflash

• QuadSPI can control 2 x 4-bit serial flashes:
  - Parallel mode enabling ‘octal flash’ with data recombination internally in QuadSPI

• Up to 100 MHz DDR x 8 => 200 MByte/sec peak bandwidth

• Flexible Buffering Scheme:
  - Sub-buffers allocated to specific masters
  - Master prioritisation
  - Pre-fetch capability
  - Suspend & resume for lower priority masters
DRAM Controller

- MAC57D5xx supports SDR and DDR2 DRAM interfaces:
  - 16-/32-bit DDR2 (320 MHz) in BGA516
  - 16-bit SDR (160 MHz target) in 208QFP/BGA516
- Direct access of CA5, GPU and graphics masters to DRAMC bypassing the QoS301
- Access controlled by local Priority Manager
Graphics Capabilities
MAC57D5xx Vector Graphic Processor, OpenVG 1.1

- Full fixed function hardware vector graphics GPU
- Hardware tessellation
  - Minimum CPU involvement
- 16x FSAA
  - Photorealistic quality
  - No performance degradation
- Multiformat rendering
  - sRGB color transformation
- High quality vector font rendering
- Standard API OpenVG 1.1
GC355 Vector Graphics Engine

GC355  VGMark  
Performance @ 320 MHz

<table>
<thead>
<tr>
<th></th>
<th>GC355</th>
<th>VGA resolution 16X AA (Frames/sec)</th>
</tr>
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<tbody>
<tr>
<td></td>
<td></td>
<td>320MHz (projected)</td>
</tr>
<tr>
<td>Tiger (rotation)</td>
<td></td>
<td>85</td>
</tr>
<tr>
<td>UI</td>
<td></td>
<td>96</td>
</tr>
<tr>
<td>Navigation</td>
<td></td>
<td>28</td>
</tr>
<tr>
<td>Flash</td>
<td></td>
<td>42</td>
</tr>
</tbody>
</table>

- Independent 2D vector GPU use cases:
  - Instrument cluster: 2D engine accelerates needles at 60 fps; 2D-ACE renders the rest of the scene
- Infotainment: UI acceleration
- Native rendering of true-type fonts, with 16x anti-aliasing
- Additional graphics acceleration for dual display systems
2D-ACE: Concept

- Real time, un-buffered screen composition
- Multiple color formats, optimized for high quality and low memory footprint
- Hardware-accelerated sprite animation, object, alpha, position, color key, scroll
- Automatic, synchronized and high latency-tolerant: needs very little CPU time
2D-ACE: Object Management
What is a layer?

- A layer is the mechanism by which graphics are displayed on the panel.
- The DCU has a set of 9 registers to configure each layer.
- The layer registers configure:
  - Height & width of layer (pixels)
  - Signed position on panel (x,y)
  - Pointer to graphic (32-bit)
  - Graphic coding (bpp) & CLUT, blending, type, tile & safety
  - Chroma limits (max & min)
  - Tile size
  - Transparency mode colors
2D-ACE: High Level Overview

- 32 layers
- 6 planes
- Up to 80 MHz pixel clock
- Memory size optimized
- Per-object animation at frame rate
- Frame buffer limited by memory size (all memories, RAM, ROM INT, EXT)
- Support 16, 24, 32 bit color depth
- Support 1, 2, 4, 8 bpp indirect color mode

- Alpha blend (per pixel & per layer in 6 planes)
- Chroma key (range per RGB component in 6 planes)
- Combined alpha blend and chroma key modes
- Font mode blending (transparency mode/alpha map)
- Highlight area mode (luminance offset)
- Tile mode
- Safety mode support
HUD Warping / Architecture

Next Gen 2D-ACE

2D ACE
- Fetch
- Blending

HUD De-warping
- Gamma
- Dithering

Memory

Plane 0-5

Warping Parameter

• Gamma
• Dithering
In-the-loop De-warping

Fetch graphic data → Blend result → Apply de-warping
HUD Warping Support / Features

Application View
• Requires setup of warping parameters (once)
• De-warping function is performed on blended output
• For the application this then looks like a regular display!
• Warping parameters can be modified during operation (VSync)

Features
• Supports invisible source pixels (i.e. destination pixels not covered by a source pixel)
• Warping parameters is usually a static table calculated offline
• DDR friendly access pattern
Video Interface Unit (VIU4)

- QVGA to XVGA input/output resolution
- Brightness and contrast adjustment
- Up to 1/8th video down-scaling
- Up to 2x horizontal video up-scaling
- Horizontal mirroring
- DMA for direct copy to system memory

<table>
<thead>
<tr>
<th>Input Formats</th>
<th>Output Formats</th>
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<tbody>
<tr>
<td>ITU-R BT.565</td>
<td>8 bpp, 16 bpp, 32 bpp</td>
</tr>
<tr>
<td>Parallel</td>
<td>8 bpp monochrome</td>
</tr>
<tr>
<td>RGB888/666/565</td>
<td>YUV422</td>
</tr>
<tr>
<td>Serial RGB888 (3 cyc)</td>
<td>YUV444</td>
</tr>
<tr>
<td>Monochrome</td>
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Safety and Security
Software and Enablement
Addressing Functional Safety and Security

- ASIL-B compliant MCUs – meets ISO26262 requirements
- Safe Assure functional safety program:
  - Safety Process - integrating functional safety into dev process
  - Safety Hardware – built in self tests, error code correction, etc
  - Safety Software – Autosar MCAL, OS, core self tests, etc
  - Safety Support – training, documentation and tech support

- Designed to support next generation security needs using Secure Boot, Secure Mileage & Component Protection
- Hardware Security Module (HSM)
  - Meets SHE Spec requirements
  - Dedicated security core
  - Secure Flash and SRAM
  - Cryptographic module – AES-128 & random number generator that helps protects security keys, secure boot up, tamper detection, advanced debug support, etc
MAC57D5xx - Enablement Support

Operating Systems & MCAL’s
- AutoSAR 4.0 MCAL & OS
- Green Hills Integrity

Drivers
- Tiny 2D API
- OpenVG1.1
- 2D-Animation Composition Engine
- Sound Generator Module
- Ethernet AVB
- IOP/Stepper Motor
- Stepper Motor Stall Detect

Compilers
- Green Hills
- ARM

Debuggers
- Lauterbach
- IAR
- Green Hills

HW Development & Reference Design
- Evaluation Board
  - 516 BGA
  - P/N & ASP TBD
- Instrument Cluster Reference Design
  - 208 LQFP
  - 176 LQFP
  - P/N & ASP TBD

User Interface Design Tools
- Altia
- ElectroBit

Flash Programming Tools
- P&E Cyclone Pro
- Promik
Summary

Industry’s highest performance, triple-core, single-chip instrument cluster solution based on ARM technology

- Freescale MAC57D5xx MCUs deliver the widest range of performance and memory expansion options to enable scalable, attention-grabbing instrument clusters

- The ARM Cortex-based MAC57D5xx triple-core MCU family offers a single chip solution with premium-level graphics capability, including heads-up display

- Freescale provides a simplified development environment for a more streamlined approach, leveraging proprietary IP and optimized code for quicker time to market