Healthcare Implementations of Wearable Technology

FTF-HCR-F0083

Dr. Jose Fernandez | Healthcare Business Development

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Session Introduction

• This session will focus on the wearable reference design for healthcare and will explain design challenges, architecture and technical system details. Subject matter experts from Freescale and hardware and software partners will be on hand to demonstrate an i.MX- and Kinetis-based design.
Session Objectives

• You will learn what a wearable device is
• Learn the characteristics of the consumer and healthcare and fitness wearables market
• Describe block diagrams of such devices, specifically for the healthcare and fitness market
• Demonstrate a standalone demo of a daughter card for a continuous heart rate monitor
• Learn the products that best suit these devices and how to achieve the key factors for these devices like low power performance and best accuracy
Agenda

• Wearable Market Description
• Market Challenge
• Freescale Wearable Reference Platform: WaRP
• Freescale and ROHM Healthcare and Fitness Daughter Board and Standalone Mode Featuring Kinetis L16 MCU
• Kinetis L16 MCU Basics
• Kinetis L16 MCU Power Saving Modes
• Demo
Wearable Market Description
The Internet of Things is Driving **Explosive Growth** In Connected Devices

*Sources: Ericsson, February 2011; Cisco Internet Business Solutions Group (IBSG), April 2011*
What Is A Wearable Device?

• Products that enhance the user’s experience as a result of the product being worn through sensing, connectivity and processing of data

Key Market Trends for Wearables:

• Miniaturization
• Low power
• Connectivity
• Multiple sensors
Austin Marathon – Freescale Survey

- 74% use wearables to train
- 88% of people surveyed said they rely on wearables for motivation similar to a coach
- 78% believe wearables give them a competitive edge
- 88% plan to use fitness wearables in the future
Fastest growing market over the next five years in both units and revenue

Sources: IHS Research, ABI Research, Credit Suisse Equity Research, Berg Insight, Juniper
## Wearable Market: Segmentation

<table>
<thead>
<tr>
<th>Vertical</th>
<th>Categories</th>
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<tbody>
<tr>
<td><strong>Fitness and Wellness</strong></td>
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<td>Healthcare and Medical</td>
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<td>Industrial and Military</td>
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Wearable Market: Diverse Usage Models

Head:
- Augmented reality
- Navigation
- In-view notifications
- Email/text (view & edit)
- Web browsing
- Photography

Wrist:
- Notifications
- Calling (place/answer)
- Fitness & health monitoring
- Navigation / Location
- Photography

Neck / Chest / Arm:
- Fitness & health monitoring
  - Calories
  - Pedometer
  - Heart rate
  - Blood pressure
  - SOS / Emergency
  - Location tracking

Leg / Ankle:
- Fitness & health monitoring
  - Calories
  - Pedometer
  - Heart rate
  - Blood pressure
  - Location tracking
Freescale serves more markets than any other supplier
• Brodest portfolio of ARM-based products in the industry
• World-class scalability and flexibility within product portfolios
• Products aligned with development needs for Internet of Things (IoT)
Market Challenge
Wearables Challenge

Power, space and usability are key

- **Space**
  Form factor and “look” are critical to success – miniaturization and fashion

- **Power Consumption**
  Extended battery life is a must as consumers will not charge their wearable device throughout the day the way they do their smart phones

- **Charging**
  USB charging is standard right now. Wireless charging is optimized for charging on flat surface. Watch design is not flat (wrist strap is the issue).

- **Usability**
  Must collect meaningful data and provide a method for intuitive and motivational use

- **Scalability**
  Market is evolving so platform must scale to adapt new capabilities
2014 WaRP Coverage Highlights

“Wearables Get their own Raspberry Pi with Freescale’s WaRP platform,” 1/6/2014


“Freescale, Partners Launch Wearable Device Reference Platform,” 1/6/2014

“Freescale Steps up Push into Wearable Technology Market,” 1/6/2014

“Freescale Wants to Kick start DIY Wearables with new WaRP Development Kit,” 1/6/2014

“Freescale Hopes to Power the Wearable Tech Trend,” 1/7/2014


“Freescale Teams up to Offer Wearable Reference Design,” 1/7/2014

“Freescale’s Wearables Reference Platform (WaRP) Supports Multiple Apps,” 1/6/2014

“CES 2014: Less is More for Smart Watches and Other Wearable Gadgets,” 1/8/2014

“Freescale’s WaRP Wearable Platform Kit Unveiled at CES,” 1/8/2014

“Reference Design Supports Simpler, Smarter Wearables,” 1/9/2014

“It Takes a WaRPed Mind to Design Wearable Tech,” 1/7/2014
Freescale Wearable Reference Platform: WaRP
Wearable Reference Platform (WaRP)

• Speeds and eases development for creating wearable devices by addressing key technology challenges which frees developers to focus on creating differentiated features:

  - Connectivity
  - Usability
  - Maximizing battery life
  - Miniaturization

Shipping June 14
Creating Wearable Innovation

| Scalable | • Modular architecture to enable rapid platform evolution |
| Key Development Challenges | • Battery life, limited space (form factor), cost and usability |
| Open Source | • Community drives innovation |
| Partnerships | • Over 15 partners |
Hardware And Software Details

Main Board PCB size:
38 mm x 14 mm
(1.49” x 0.55”)

Daughter Board PCB size:
42 mm x 42 mm
(1.65” x 1.65”)

**BATTERY SINGLE CELL LIPO**
(500mAh)

**POWER MANAGEMENT**
Maxim MAX77696

**MEMORY**
LPDDR2 + eMMC
Samsung MCP KMN5W000ZM-B207

**i.MX 6SL**
ARM® Cortex™-A9 Apps Processor Running Android

**MIPI-DSI**
Solomon SSD2805

**3-axis ACCELERO**
3-axis MAGNETO
FXOS8700CQ

**W-LAN / BLUETOOTH 4.0**
Murata LBEH17YSHC

**BOARD - TO - BOARD CONNECTOR**

**HUB SENSOR**
MCU – Kinetis KL16
ARM® Cortex™ M0+

**MOTION SENSING**
Pedometer
MMA9553

**WIRELESS CHARGING**

**BOARD - TO - BOARD CONNECTOR**

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**WIRELESS CHARGING**

**BOARD - TO - BOARD CONNECTOR**
Processor Selection: MCUs vs. Apps Processors

- MCUs targeted towards simplified, single function solutions
- MPUs provide higher performance, ability to run a full operating system and support multiple functions
- A hybrid approach addresses the diversity of the devices being covered by this reference platform
- A hybrid designs allows for optimized power management to extend battery. The ability to scale the power requirements is necessary to achieve longer battery life through power-down and sleep mechanisms.
- This approach allows for a smaller footprint without compromising the ability to scale the solution to multiple performance tiers
Hardware Overview

• Main board (APB) based on i.MX 6SoloLite applications processor runs Android and provides:
  - Bluetooth and Wi-Fi 802.11
  - Power Management - Integrated Lipo charger
  - 6-axis Accelerometer and Mag sensor
  - Supports LCD and E-ink display
  - Micro USB OTG for host USB and device power / battery charging
  - Daughter board expansion interface

• User replaceable daughter board for expansion, based on Freescale Kinetis L Series MCU
  - Pedometer functionality with Freescale’s MMA9553L sensor
  - Wireless charging
  - User interface buttons
Application Examples

- Time, chrono, lap time, alarms
- Smart music player with audio streaming to headset
- Photo and video player
- Bluetooth Smart and Wi-Fi connectivity
- Compass
- Free fall detection
- Pedometer / activity monitor
- Step counter (pedometer)
- Motion detection (walking, running)
- Distance traveled
- Calories
- ECG and heart rate monitoring
- Wake up on motion
- Charging over USB
- Wireless charging
WaRP Hardware Architecture

• Open source platform – design files available
• Hybrid architecture for optimized power management
  – Main processor only on when needed for connectivity or display update
  – Low power MCU for sensor monitoring on all the time
• Power management
• Small form factor through tight design
  – Details to provide on PCB
• Flexibility in display options
  – Standard LCD
  – Eink display – low power
• Dual-mode connectivity
  – Wi-Fi for direct connectivity to a hub -> cloud
  – Bluetooth Smart for tethering to a smart phone
Freescale’s Wireless Charging Solutions

Broad Flexibility
• Industry’s first programmable solution, offering customers the utmost design flexibility

Accelerate Time-to-Market
• Production-ready designs with market specific focus

Unequivocal Performance
• Unparalleled performance delivering an optimized HW and SW platform
Wearables Wireless Charging Reference Design

Features

• Kinetis MCU to drive sensors and wireless charging receiver
• i.MX 6SoloLite applications processor for connectivity, user interface and power management
• Reference platform providing fully featured hardware platform to develop differentiated product

Target applications

• Smart watches, fitness gear, medical devices, etc.
• Wireless charging receiver functionality via Kinetis MCU to provide – 5 Watts
WaRP: Software Architecture and Completeness

Applications

<table>
<thead>
<tr>
<th>UI</th>
<th>Apps</th>
<th>Launcher</th>
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Segment Specific

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<tr>
<th>Infotainment</th>
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<tr>
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<td>• ECG/HR</td>
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<tr>
<td>• Wearable gaming</td>
<td>• Compass</td>
<td>• Glucometer</td>
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<tr>
<td>• Music</td>
<td>• Motion Sensing</td>
<td>• Skin thermometer</td>
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<tr>
<td>• Video</td>
<td>• Body Activity Monitor</td>
<td>• Data Aggregation</td>
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</tbody>
</table>

API

| • Android Standard API | • Device Specific API | • Bluetooth Profiles | • Custom Third Party API |

OS Layer

| • Power Management | • Bootloader | • Core stacks |
| • Bluetooth Core Stack | • Kernel |  |
| • Video Codecs | • Drivers |  |
| • Kernel 3.0.35/3.5.x |  |  |
| • Device Drivers |  |  |
| • Microcontroller Access Protocol |  |  |

Hardware

Application Processor: i.MX 6SoloLite
Microcontroller: Kinetis L Series
i.MX Android Leadership

- **Commitment:** 9 Android OS versions released over past 7 years
- **Broad Acceptance:** 25,000+ downloads of BSP to date
- **Fast Development:** ~4 months from development start to production release on multiple Android versions
- **Cross market robustness:** Automotive, Embedded/Industrial, Consumer
- **Continued support:** New OS releases for 2 years after silicon production qual
- **Leadership:** i.MX – only Android system shipping in a top 5 OEM infotainment platform today
WaRP Software Implementation

• Why Android?
  - Wearable device purpose: collect data and pass that data to hub/cloud
  - Wearables evolving from single-function to multi-function requires rich ecosystem of app developers
  - User Interface extensive capabilities
  - Full connectivity stack: BT/Wifi allows the wearable device be connected to Cloud Services
  - Android Recovery System to update the OS with new features or install new software updates

• WaRP Android software advantages
  - All implemented within standard Android SDK framework so developers can still use the Android software development kit for app development
  - WaRP main board can be a standalone wearable computer
  - Provides software examples to enable LCD or eInk graphic UI to speed up development and prototyping phases and get to market quicker
  - Simple interface to daughter card to pull in date from sensors

• Open source Android platform with exception of 3rd part components – Vivante graphics and QCA Wi-Fi
• Full Android BSP with 3rd party components available via click-through license
Time And Date Profile

• **Long operating time, no data-intensive processing**

• **Key Functions**
  - Update time
  - Monitor GPIO
  - Notifications/alerts

• **Expectations**
  - Long battery life
  - Ideally never wake up Cortex-A core during updating just time

• **Power Profile**
  - TBD
i.MX 6SoloLite Multimedia Processor

**Specifications**
- CPU: 1x ARM® Cortex®-A9 @ 1GHz
- Process: 40nm
- Core Voltage: 1.1V
- Package: 0.5mm 13x13 MAPBGA

**Key Features and Advantages**
- High performance ARM Cortex-A9 up to 1GHz with 256KB L2 cache
- x32 LP-DDR2, DDR3/LV-DDR3 and managed NAND support
- Flexible display options for next gen solutions
  - Integrated EPD controller
  - LCD Display up to WXGA (1366x768)
- 3 USB 2.0 support with 2 integrated PHY, x1 HSIC
- Audio Interfaces include I2S/SSI, S/PDIF Tx/Rx

### System Control
- Secure JTAG
- PLL, Osc
- Clock & Reset
- Smart DMA
- IOMUX
- Timer x3
- PWM x4
- Watch Dog x2

### Power Mgmt
- LDO
- Temp Monitor

### Internal Memory
- ROM
- RAM

### Security
- HAB
- Secure RTC

### ConnectivityManager
- MMC 4.4 / SD 3.0 x3
- MMC 4.4 / SDXC
- UART x5
- I²C x3, SPI x4
- USB2 OTG & PHY
- USB2 Host & PHY
- USB2 HSIC Host
- 10/100 Ethernet
- SMBus, GPIO, Keypad
- I²S/SSI x3
- S/PDIF Tx/Rx

### Internal Memory
- X32 LP-DDR2, DDR3 / LV-DDR3

### CPU Platform
- 1x Cortex-A9
- 32KB I-cache
- 32KB D-cache
- NEON
- PTM
- 256KB L2-cache

### Graphics
- GPU2D: OpenVG1.1
- CSC, Combine, Rotate, Gamma Mapping

### EPDC
- E-INK™ Panels w/IF

### LCD & Camera Interfaces
- 24-bit RGB
- 16-bit Parallel CSI

### Connectivity
- MMC 4.4 / SD 3.0 x3
- MMC 4.4 / SDXC
- UART x5
- I²C x3, SPI x4
- USB2 OTG & PHY
- USB2 Host & PHY
- USB2 HSIC Host
- 10/100 Ethernet
- SMBus, GPIO, Keypad
- I²S/SSI x3
- S/PDIF Tx/Rx
### i.MX 6 Series Processors At A Glance

**Scalable series of five ARM Cortex A9-based SoC families**

#### i.MX 6SoloLite
- Single ARM® Cortex™-A9 at 1.0GHz
- 256KB L2 cache, Neon, VFPvd16, Trustzone
- 2D graphics
- 32-bit DDR3 and LPDDR2 at 400MHz
- Integrated EPD controller

#### i.MX 6Solo
- Single ARM Cortex-A9 at 1.0GHz
- **512KB** L2 cache, Neon, VFPvd16, Trustzone
- **3D graphics** with 1 shader
- 2D graphics
- 32-bit DDR3 and LPDDR2 at 400MHz
- Integrated EPD controller

#### i.MX 6DualLite
- **Dual** ARM Cortex-A9 at 1.0GHz
- 512KB L2 cache, Neon, VFPvd16, Trustzone
- **3D graphics** with 1 shader
- 2D graphics
- 64-bit DDR3 and 2-channel 32-bit LPDDR2 at 400MHz
- Integrated EPD controller

#### i.MX 6Dual
- **Dual** ARM Cortex-A9 at 1/1.2GHz
- 1 MB L2 cache, Neon, VFPvd16, Trustzone
- 3D graphics with 4 shaders
- **Two** 2D graphics engines
- 64-bit DDR3 and 2-channel 32-bit LPDDR2 at 533MHz
- Integrated SATA-II

#### i.MX 6Quad
- **Quad** ARM Cortex-A9 at 1.2GHz
- 1 MB L2 cache, Neon, VFPvd16, Trustzone
- 3D graphics with 4 shaders
- Two 2D graphics engines
- 64-bit DDR3 and 2-channel 32-bit LPDDR2 at 533MHz
- Integrated SATA-II

### Pin-to-Pin and Power Compatible

### Software Compatible

- ARM Cortex-A9 based solutions ranging up to 1.2GHz
- HD 1080p encode and decode (except 6SL)
- 3D video playback in High definition (except 6SL)
- SW support: Google Android™, Windows® Embedded CE, Linux®

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**Features vary by product family**
Xtrinsic FXOS8700CQ 6DOF eCompass Sensor

Low noise, low offset 3-axis accelerometer + magnetometer eCompass sensor enabling <5° absolute heading accuracy and ±0.1° resolution performance

Differentiating Points

• 14b data gcell ADC with 33% lower noise and 3x lower offset
• 16b data mcell ADC with 0.6 uT-rms noise density
• Vector magnitude change detection for faster system response and lower power
• Autonomous hard iron calibration
• Production-ready calibration and award winning eCompass software
• Pin compatible with Freescale accelerometer portfolio

Product Features

• 1.95 – 3.6V supply, 1.6 – 3.6V I/O
• ±2g/±4g/±8g FS accelerometer range
• ±1200 µT FS magnetometer range
• Output data rate (ODR) from 1.563Hz to 800Hz, 400Hz hybrid
• Flexible motion detection functions (e.g., freefall, pulse, transient, tap)
• 3 x 3 x 1.2mm QFN Package

Typical Applications

- Electronic compass
- Scientific: Aurora detection
- Industrial: Directional drilling, mineral exploration, parking detection
- GPS assist for Location Based Services
Xtrinsic MMA955xL

3-Axis Accelerometer plus 32-bit ColdFire MCU

Differentiating Points
• Intelligent Motion Platform with embedded libraries
• Sensor hub capability
• Power management features and low power modes

Product Features
• 1.71 to 1.89V supply voltage
• Output data rate (ODR) 488 Hz
• +/-2g, 4g, 8g configurable dynamic ranges available
• 14/12/10/8 bit resolution available
• 16K Flash, 2K RAM
• 3x3x1mm LGA, 0.5mm pitch

Typical Applications
• Mobile: phones, tablets, eReaders
• Controllers: remotes, games
• Sports monitoring
Xtrinsic MMA955xL Variations

• MMA9550L
  - Infrastructure only functions
  - User Flash: 6.5 Kbytes
  - User RAM: 576 bytes

• MMA9551L
  - Infrastructure plus gestures
  - User Flash: 4.5 Kbytes
  - User RAM: 452 bytes

• MMA9553L
  - Infrastructure plus pedometer
  - User Flash: 1.5 Kbytes
  - User RAM: 200 bytes

• MMA9559L
  - Lightweight Infrastructure
  - User Flash: 14 Kbytes
  - User RAM: 1.5 bytes
Kinetis L Series MCUs: Low Power Pillars

**Ultra-efficient Cortex-M0+ processor**
- Most energy-efficient 32-bit processor on the market with industry leading throughput/mA

**Energy-saving architecture**
- Optimized for low power with 90nm TFS technology, clock and power gating techniques, and highly efficient platform featuring a low power boot option, bit manipulation engine, peripheral bridge crossbar and zero wait state flash memory controller

**Ultra-low power modes**
- Several, flexible power modes fit for different application use cases designed to maximize battery life

**Energy-saving peripherals**
- Smart peripherals with functionality in deep sleep modes can make intelligent decisions and process data without waking up the core
5W Embedded Receiver Concept

**Target Applications**
- Smart Watches
- Mobile Medical Devices
- Fitness Monitors
- Mobile Phones
- Smart Phone Accessories

- Wireless charging with minimal cost adder
- Remove the need for a separate wireless charging ASIC
- Can be implemented in any device with an embedded Freescale MCU
- Lowest system BOM cost compared to existing implementations
Partner Components

• Murata LBEH17YSHC Wi-Fi® (802.11 b/g/n) and Bluetooth® (4.0 BLE + EDR) Wireless Module

• Samsung MCP KMN5W000ZM-B207 – LPDDR2 and eMMC

• Maxim MAX77696 Power Management IC – integration provides for board space savings

• Eink EPD (ET017QC1) and LCD (LH154Q01) display options – LCD supports capacitive touch

• Battery
Freescale and ROHM Healthcare Fitness Daughter Board and Standalone Mode Featuring Kinetis L16 MCU
Continuous Heart Rate Monitor

Healthcare and Fitness

- The heart rate module measures the amount of blood flowing through a vessel by emitting light and measuring its reflection through the optical sensor. The Analog Front End filters, amplifies and processes the analog signal and presents it to the MCU in adequate levels.

- There are two main algorithms:
  - Steady patient mode
  - Exercising mode
Continuous Heart Rate Monitors

• Are used for healthcare and fitness applications in which the heart rate needs to be continuously monitored to be kept in, within certain parameters. i.e.:
  – Exercising for burning fat
  – Exercising for cardiovascular training
  – For health conditions in which we don’t want to go over the maximum heart rate (elderly patients, arrhythmia patients, etc)
WaRP Board with Heart Rate Daughter Board

Main Board PCB size: 38 mm x 14 mm (1.49" x 0.55")
Block Diagram in Detail

Wearable HRM

Blood Vessel

Optical Sensor

Analog Front End

Microcontroller MKL15Z128VFM4

Accelerometer KX022-1020

NFC RC-S802

Power Supply

Analog Data

PWM

DAC

EEPROM (TBD, Optional)

WaRP Connector

User Interface

Serial Communications (SONY Proprietary)

I2C/SPI

Optical Signals

Data signals

Power

User Feedback

Freescale WaRP

User

WaRP Board with Heart Rate Daughter Board
Kinetis KL1x MCU Family: Block Diagram

- **ARM® Cortex™-M0+ Core**: Debug Interfaces, Interrupt Controller, Micro Trace Buffer. 48 MHz.
- **System**: Internal Watchdog, DMA, Low-Leakage Wake-Up Unit, Bit Manipulation Engine, Unique ID.
- **Memories**: Program Flash (32 to 256 KB), SRAM (4 to 32 KB).
- **Clocks**: Phase-Locked Loop, Frequency-Locked Loop, Low/High-Frequency Oscillators, Internal Reference Clocks.

- **Analog**: 16-bit ADC, Analog Comparator, 12-bit DAC.
- **Timers**: PWM, Periodic Interrupt Timers, Low-Power Timer, Real-Time Clock.
- **Communication Interfaces**: 2x I²C, Low-Power UART, 2x UART, 2x SPI, I²S.
- **HMI**: GPIO, Xtrinsic Low-Power Touch-Sensing Interface.

Options: Standard, Optional.
Layout Heart Rate Daughter Board

Top View - With Battery and NFC

- NFC Module
- Battery Pack

Top View - Without battery and NFC module

- Microcontroller
- Accelerometer
- Push Button
- Programming Connector
- Serial Connector
- Reset Button
- Charging Port
- ON/OFF Switch
- RGB LED (Heart Rate)
- Red LED (Battery Charge)

NOTE: Push Buttons are pressed on the lateral side
Kinetis L16 MCU Basics
Kinetis L Series MCUs:
Enabling Differentiation in Entry-Level Products

Energy efficiency
Class-leading
CoreMark/mW

Scalability and integration
Kinetis L to K Series
MCUs (ARM Cortex-M0+ to Cortex-M4)

Enablement
Freescale bundle +
ARM ecosystem

Ultra-low static
<1uA

Low cost
From <$0.50

Ease of use
Freedom Platform,
Processor Expert and
MCU Solution Advisor

Kinetis L Series MCUs
The evolution of the entry-level MCU
Kinetis L Series MCUs: Target Applications

Banking
- OTP
- Cash Registers

Building Control
- Smoke Detector
- Thermostat

Instrumentation & Medical
- Joy Sticks
- Remote Controller
- Aero Model
- Scale
- Shaver
- Mouse
- GPS Watch

Mass Market
- ETC
- Electronic Label
- Fiber Module
- RFID

Mass Market

Energy Efficiency
Leading Next-Generation 32-bit Development

Freescale and ARM collaborated to develop a revolutionary processor that extends battery life by improving energy efficiency, enables advanced peripherals and software by increasing processing performance and reduces system cost by improving code density.

Freescale’s MCU experts helped define key ‘8-bit-like’ processor features including ease of use.

Cortex-M0+ processor successfully integrated into first Kinetis L series MCU platform—now available.

Freescale general embedded MCU roadmap fully aligned with Cortex architecture from entry-level Kinetis L series MCUs to high-performance Kinetis K series MCUs with broad performance, memory and feature scalability.
## Benefits of Moving from 8-/16-bit Architecture to a 32-bit Architecture Built on the ARM Cortex-M0+ Processor

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<th>8-/16-bit</th>
<th>32-bit ARM Cortex-M0+</th>
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<tr>
<td><strong>Performance</strong></td>
<td><strong>Performance</strong></td>
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<tr>
<td>• Older, slower architectures and technology</td>
<td>• 2x to 40x more than 8/16-bit, 9% more than Cortex-M0</td>
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<tr>
<td>• Increased code size/complexity when performing complex math operations</td>
<td>• Fast 32-bit math processing</td>
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<tr>
<td>• Fast single-cycle access to I/O</td>
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<tr>
<td><strong>Energy efficiency</strong></td>
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<tr>
<td>• Low energy efficiency</td>
<td>• &gt;2x CoreMark/mA than closest 8/16-bit MCU, +30%/CM0</td>
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<tr>
<td><strong>Low cost</strong></td>
<td><strong>Low cost</strong></td>
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<tr>
<td>• 6-35 kgates</td>
<td>• 12-35 kgates</td>
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<tr>
<td>• Variable code density</td>
<td>• Excellent code density</td>
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<tr>
<td><strong>Ease of development</strong></td>
<td><strong>Ease of development</strong></td>
</tr>
<tr>
<td>• Limited addressable memory</td>
<td>• Linear 4 GB address space—no need for paging</td>
</tr>
<tr>
<td>• Simplistic interrupt controllers</td>
<td>• Full-featured interrupt controller—simpler s/w architecture</td>
</tr>
<tr>
<td>• Limited scalability (MHz, flash, features)</td>
<td>• Huge scalability—h/w and s/w reuse across end products</td>
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<tr>
<td>• Limited ecosystem support</td>
<td>• Huge ARM ecosystem—off-the-shelf software/tools/training</td>
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<td></td>
<td>• Micro Trace Buffer—lightweight, non-intrusive trace</td>
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The ARM Cortex-M0+ Processor

Shorter Pipeline
Optimized for Energy Efficiency

Full ARMv6-M Compatible

More Options

- From Cortex-M3
- Re-locatable Vector Table
- Memory Protection Unit (MPU)
- Fast I/O Port
- Micro Trace Buffer (MTB)
The ARM Cortex-M0+ Processor

Energy Efficiency

• 2-stage pipeline—reduced cycles per instruction (CPI), enabling faster branch instruction and ISR entry
• Program memory access on alternate cycles

Single-Cycle I/O Port

• 50% higher GPIO toggling frequency than standard I/O
• Improves reaction time to external events, allowing bit-banding and software protocol emulation
• Save precious cycles (e.g., set faster peripherals for low-power access)
• Access GPIO/peripherals while processor fetches the next instruction

Processing

• Only 56 Instructions, mostly coded on 16-bit. Option for fast MUL 32x32 bit in 1 cycle.
• Cortex-M0/3/4 compatible
• 1.77 CM/MHz
• Best-in-class code density vs. 8/16-bit architectures—reduced cost, power consumption and pin-count

Micro Trace Buffer

• Powerful, lightweight trace solution, enabling fast debug
• Non-intrusive—trace information stored in small area of MCU SRAM (size defined by programmer)
• Trace read over Serial Wire/JTAG (CPU stopped)
The ARM Cortex-M0+ Processor That Enables Kinetis L Series MCUs

- Bit Manipulation Engine
- Integration
- 90 nm TFS Memory
- Flash Memory Controller
- Micro Trace Buffer
- eDMA Crossbar
- RGPIO

Smart Evolution *Instead of Revolution*

- Reduce # of Cycles
- Reduce Overall Power Consumption
- Comprehensive Compatibility
- Improved Performance
- Autonomous & Precise Low-Power Peripherals
The ARM Cortex-M0+ Processor: Low Power by Design

Dedicated features built in the processor:

- **WFI & WFE instructions:** set core into **sleep** and **wait-for-event/interrupt**
- **Sleep-on-exit:** automatic **sleep** after interrupt execution
- Few cycles to switch between run and sleep

Deep sleep for longer sleep period:

- CPU and NVIC unpowered or in SRPG
- WIC monitors wake-up sources
- Static processor leakage in nW

Kinetis L Series MCUs implementation:

- Asynchronous WIC (**AWIC**)
- Multiple WU sources: periph/LV/NMI
- Additional **LLWU** for low-leakage wake-up
The ARM Cortex-M0+ Processor: Code Efficiency

- ARMv6-M Thumb Instruction Set
  - 32-bit performance at 16-bit density
- 32-bit Simplification
  - 32-bit data structure
  - 32-bit Address Space (no paging)

### ARM Cortex-M0+ Processor

- **ARMv6-M Thumb Instruction Set**
  - 32-bit performance at 16-bit density

#### 32-bit Simplification

- 32-bit data structure
- 32-bit Address Space (no paging)

### 16-bit Multiplication Example

<table>
<thead>
<tr>
<th>3-bit example</th>
<th>16-bit example</th>
<th>ARM Cortex-M4</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOV A, #12</td>
<td>MOV A, #1</td>
<td>MOV A, #12</td>
</tr>
<tr>
<td>MOV B, #3</td>
<td>ADD A, R1</td>
<td>MOV B, #3</td>
</tr>
<tr>
<td>MOV A, #1</td>
<td>MOV R1, A</td>
<td>MOV A, #1</td>
</tr>
<tr>
<td>MOV R0, A</td>
<td>MOV A, #2</td>
<td>MOV R0, A</td>
</tr>
<tr>
<td>MOV B, #2</td>
<td>MOV A, #1</td>
<td>MOV B, #2</td>
</tr>
<tr>
<td>MOV A, #12</td>
<td>MOV B, #1</td>
<td>MOV A, #12</td>
</tr>
<tr>
<td>MOV B, #3</td>
<td>ADD B, R2</td>
<td>MOV B, #3</td>
</tr>
<tr>
<td>ADDC A, R1</td>
<td>MOV A, #1</td>
<td>ADDC A, R1</td>
</tr>
<tr>
<td>MOV R1, A</td>
<td>MOV B, #2</td>
<td>MOV R1, A</td>
</tr>
<tr>
<td>MOV A, #2</td>
<td>MOV A, #1</td>
<td>MOV A, #2</td>
</tr>
<tr>
<td>ADDC A, #2</td>
<td>MOV B, #2</td>
<td>ADDC A, #2</td>
</tr>
<tr>
<td>MOV R2, A</td>
<td>MOV A, #1</td>
<td>MOV R2, A</td>
</tr>
<tr>
<td>MOV A, #3</td>
<td>MOV R0, A</td>
<td>MOV A, #3</td>
</tr>
<tr>
<td>MOV B, #3</td>
<td>MOV B, #2</td>
<td>MOV B, #3</td>
</tr>
</tbody>
</table>

- **1cycle**
- **2Byte Code Size**

### CoreMark Code in kB

- Code compiled optimized for size

**Cortex-M0+**

- **A (16-bit)**: 10,206
- **B (16-bit)**: 10,066
- **C (8-bit)**: 6,446
- **D (8/16-bit)**: 5,418

---

Note: The Cortex-M4 multiply instruction performs a 32-bit multiply, hence we assume 0 and 1 contain 16-bit data.
The ARM Cortex-M0+ Processor:
No compromise in performance

Shorten run time in low-power applications

- **More than 2x CoreMark/mA performance** than the closest 8/16-bit competitor
- **2-stage pipeline**—reduced number of cycles per instruction (CPI) enables faster branch instruction and ISR entry, reduced power consumption and increased performance
- **Fast I/O port**—single-cycle access to I/O (2x faster than normal I/O)
  - Improves reaction time to external events, allowing bit-banding and software protocol emulation
  - Implemented as FGPIO on Kinetis L series MCUs

Official data: www.coremark.org
Kinetis L Series MCUs:
Reduce cycles with parallelization and acceleration schemes

- Support concurrent access from DMA/core to memory and peripherals—offload CPU
- Kinetis L series MCUs support DMA operation in low-power modes

Any operation involving a DMA channel follows the same three steps:
1. Channel initialization
2. Data transfer
3. Channel termination

The FMC supports 8-bit, 16-bit and 32-bit read operations from the program flash memory.

In addition, the FMC provides two separate mechanisms for accelerating the interface between bus masters and program flash memory. A 32-bit speculation buffer can prefetch the next 32-bit flash memory location and a 4-way, 4-set program flash memory cache.
Freescale Bit Manipulation Engine (BME) provides hardware support for atomic read-modify-write memory operations to the peripheral address space in Cortex-M0+-based microcontrollers. This architectural capability is also known as "decorated storage.”

Resides between a crossbar switch slave port and a peripheral bridge bus controller.

Decorated loads support unsigned bit field extracts, load- and- {set, clear} -1bit Operations.

Decorated stores **support bit field inserts, logical AND, OR and XOR operations**. Support for byte, half word and word-sized decorated operations.

For most BME commands, a single-core read or write bus cycle is converted into an atomic read-modify-write, that is, an indivisible “read followed by a write” bus sequence.

Bit Manipulation Engine (BME)
Decorated load and store capability for peripherals, improving processing efficiency and small code size.

- Decorated Stores
  - AND, OR, XOR and Bit field insert (BFI)
- Decorated Loads
  - Load and clear one bit (LAC1),
  - Load and Set one bit (LAS1),
  - Unsigned bit field extract (UBFX)
Kinetics L Series MCUs:
Reduce cycles for optimized power efficiency

Supported operations
- Decorated Stores
- Logical AND, OR, XOR
- Bit field insert (BFI)

<table>
<thead>
<tr>
<th>Task</th>
<th>Normal C Code Size</th>
<th>BME Code Size</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logical XOR operation</td>
<td>12Bytes</td>
<td>6Bytes</td>
<td>50%</td>
</tr>
<tr>
<td>Bit Field Insert</td>
<td>24Bytes</td>
<td>6Bytes</td>
<td>75%</td>
</tr>
</tbody>
</table>

GPIOA_PDOR ^= 0x02; // Logical XOR

```c
#define BME_XOR_ADDR(ADDR)  (*(volatile uint32_t *)((uint32_t)ADDR | (3<<26)))

BME_XOR_ADDR(&GPIOA_PDOR) = 0x02;
```

Uses 12 Bytes

// Macro used to generate hardcoded XOR address

```c
#define BME_XOR_ADDR(ADDR)  (*(volatile uint32_t *)((uint32_t)ADDR | (3<<26)))

BME_XOR_ADDR(GPIA_PDOR) = 0x02;
```

Uses 6 Bytes
The ARM Cortex-M0+ Processor: Fast I/O Port

**ARM Cortex-M0+ fast I/O port**
- Single-access processor
- Most suited to critical GPIO

**Advantages for the application**
- Higher GPIO toggling frequency
- Bit-bang the I/O as on a 8-bit
- Save precious cycles (e.g. set GPIO faster for low power)
- “Harvard-like:” access GPIO while processor fetches the next instruction
The ARM Cortex-M0+ Processor:
A faster route to a bug-free application

ARM Micro Trace Buffer (MTB)
- Lightweight trace
- Trace stored in RAM
- Nonintrusive
- Read over serial wire/JTAG

Freescale extensions:
- Additional address (and optionally data) watch points
- Define specific memory references were the trace start and stop

![Diagram of ARM Cortex-M0+ Processor with MTB Controller and SRAM connections](image)
Kinetis L Series MCUs Built on the ARM Cortex-M0+ Processor
Six Months from Core Licensing to MCU Production

<table>
<thead>
<tr>
<th>2012</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mar</td>
</tr>
</tbody>
</table>

**Licensed Cortex-M0+ Processor**
- World’s first ARM Cortex-M0+-based MCU
- A true 8- and 16-bit alternative
- Kinetis scalability from entry level to CM4 w/ DSP

**Announced Kinetis L Series MCUs**
- Roadmap public
- Alpha customers engaged
- Benchmark energy-efficiency proven

**In production Kinetis L Series MCUs**
- Production-qualified MCUs
- $12/€10 Freescale Freedom development platform with IDE/RTOS bundle
- Mass market engagement via global e-tailers and distributors

- Freescale logos and license logos
Kinetis: A Scalable Portfolio
Production-qualified Cortex-M0+ and Cortex-M4 MCUs

- **Kinetis K Series**
  - Cortex-M4
  - 50–150 MHz

- **Kinetis L Series**
  - Cortex-M0+
  - 48 MHz

- **K10 Family**
  - 50–120 MHz
  - 32 KB–1 MB
  - General Purpose

- **K20 Family**
  - 50–120 MHz
  - 32 KB–1 MB
  - USB OTG (FS/HS)

- **K21 Family**
  - 32 KB

- **K22 Family**
  - 32–256 KB

- **K30 Family**
  - 72–100 MHz
  - 64–512 KB
  - Segment LCD

- **K31 Family**
  - 64–256 KB

- **K40 Family**
  - 72–100 MHz
  - 64–512 KB
  - USB OTG (FS), SLCD

- **K41 Family**
  - 128–256 KB

- **K42 Family**
  - 128–256 KB
  - USB OTG (FS), SLCD

- **K50 Family**
  - 72–100 MHz
  - 28–512 KB
  - Analogue, USB OTG (FS), E’net, SLCD, Encryption

- **K60 Family**
  - 100–150 MHz
  - 512 KB–1 MB
  - Ethernet, USB OTG (FS/HS), Encryption, Tamper, DRAM

- **K70 Family**
  - 120/150 MHz
  - 512 KB–1 MB
  - Graphics LCD, Ethernet, USB (FS/HS) Encryption, Tamper Detect, DRAM

- **K80 Family**
  - 100–150 MHz
  - 512 KB–1 MB
  - Ethernet, USB (FS/HS) Encryption, Tamper, DRAM

- **K90 Family**
  - 120/150 MHz
  - 512 KB–1 MB
  - Graphics LCD, USB (FS/HS) Encryption, Tamper, DRAM

Pin Count:
- 16 pin
- 32 pin
- 48 pin
- 64 pin
- 80 pin
- 100 pin
- 121 pin
- 144 pin
- 256 pin

**KL0 Family**
- 8–32 KB, 8-bit compatible
- From $0.49

**KL1 Family**
- 32–256 KB, General Purpose
- From $0.90

**KL2 Family**
- 32–256 KB, USB OTG (FS)
- From $1.22

**KL3 Family**
- 64–256 KB, SLCD
- From $1.71

**KL4 Family**
- 64–256 KB, SLCD
- From $2.34

**KL5 Family**
- 128–256 KB, USB OTG (FS), SLCD

**KL6 Family**
- 256 KB–1 MB
- Ethernet, USB OTG (FS/HS), Encryption, Tamper, DRAM

**KL7 Family**
- 256 KB–1 MB
- Ethernet, USB (FS/HS) Encryption, Tamper, DRAM

10K# Suggested Resale Prices shown

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External Use | 62
Kinetis L16 MCU
Power Saving Modes
Kinetis L Series MCUs: Energy Efficiency

**Ultra-efficient processing**
- Cortex-M0+ processor
- 90 nm low-power flash technology
- Bit manipulation engine
- <40 uA/MHz, 4.8 CM/mW
- Peripheral bridge crossbar
- Zero wait state Flash memory controller

**Ultra low-power modes**
- 90nm low-leakage flash technology
- Multiple run, wait and stop modes
- 4 us wake-up from deep sleep modes
- Clock & power gating, low-power boot options
- 2 uA deep sleep Idd with register retention, LVD active and 4.3 us wake-up

**Energy-saving peripherals**
- Smart peripherals function in deep sleep modes and can make intelligent decisions and process data without waking up the core—ADMA, UART, timers, ADC, segment LCD, touch sensing...

Most Innovative Process Technology
Kinetis ARM Cortex-M4 MCUs
Kinetis L Series MCUs: World’s Most Energy-Efficient MCUs

- **Ultra-efficient ARM Cortex-M0+ core**
  - Very low power run at 40 μA/MHz
- **Flexible ultra-low-power modes**
  - Deep sleep down to 150 nA
- **Energy-saving architecture**
  - DMA, UART, ADC, Timers plus other peripherals functional in deep sleep

![Graph comparing MCU CoreMark/mA](image)

- Freescale KL02
  - 15.92 x 1.8
- ST Micro STM8
  - 8.84
- Microchip PIC24
  - 8.0
- TI MSP430
  - 2.1
- Renesas RL78
  - 1.9

External Use | 65
Kinetis L Series MCUs: Low-Power Pillars

Ultra-efficient ARM Cortex-M0+ processor
Most energy-efficient 32-bit processor on the market with industry leading throughput/mA

Energy-saving architecture
Optimized for low power with 90 nm TFS technology, clock and power gating techniques and a highly efficient platform, featuring a low-power boot option, bit manipulation engine, peripheral bridge crossbar and zero wait state flash memory controller

Ultra-low-power modes
Several flexible power modes fit for different application use cases designed to maximize battery life

Energy-saving peripherals
Smart peripherals with functionality in deep sleep modes can make intelligent decisions and process data without waking up the core
Energy Efficiency: Energy = Power x Time

Very Low Active and Standby Power Consumption

Energy-Saving Peripherals

Reduced Processing Time

Initialization

Control

Compute

Ultra-low Active Current

Ultra-low Standby Current

Deep Sleep Mode

RUN @3 V, 48 MHz  79 uA/MHz
VLPR @3 V, 4 MHz  39 uA/MHz
VLLS0 Deep Sleep @3V  139 nA
LLS Deep Sleep @3V  1.7 uA
CoreMark/MHz  1.77
LLS Wake-up Time  4.3 us
Ultra-Efficient ARM Cortex-M0+ Processor

Most energy-efficient 32-bit processor on the market

- Processor power consumption as low as 9 uA/MHz
  - 30% power reduction from Cortex-M0
  - 56% increased energy efficiency from Cortex-M0

- Outstanding performance results of 1.77 CoreMark/MHz
  - 2 to 40 times higher performance compared to 8/16-bit architectures, including TI MSP430, Microchip PIC18 & PIC24, and Atmel ATXmega
  - 9% increased performance from Cortex-M0

- Single-cycle fast I/O access port facilitates bit-banging and software protocol emulation, keeping an 8-bit ‘look and feel’
  - Up to 50% faster than normal I/O

- Single-cycle 32b x 32b multiply instruction

- Interrupt latency decreased by 1 cycle
Energy-Saving Architecture (1)

90 nm Thin-Film Storage (TFS) Technology
• 1/3 dynamic power reduction vs. existing technologies
• Flash support for low power modes and fast program/erase times
• Flash disable option when executing from SRAM
• Flash doze option to disable during Wait mode (adds ~1 us wake-up)

Clock and Power Gating
• Peripheral clocks are disabled by default so there is no wasted power consumption
• LLS and VLLSx modes shutdown power to most logic maintaining power to energy-efficient peripherals and wake-up sources
• Automatic platform clocking control in Compute Operation and Partial STOP options further reducing dynamic power consumption
Energy-Saving Architecture (2)

Low-Power I/O Pin Configuration
• I/O pins default to a low-power configuration, disconnecting pin from digital logic and eliminating need to configure unused I/O pins to reduce pin leakage.

Low-Power Boot Option
• Configurable power-on reset and low-power recovery time to eliminate power spikes

Bit Manipulation Engine (BME)
• Intelligent load and store capability for peripheral improved cycle count and smaller code size
Energy-Saving Architecture (3)

Peripheral Bridge Crossbar (AXBS-Lite)

• Support for concurrent accesses from masters (Core and DMA) to slaves (memory and peripherals)

Flash Memory Controller (FMC)

• 4-way, 4-set 32-bit flash cache for reducing flash accesses and eliminating wait states
# Ultra-Low-Power Modes

Expands beyond typical run, sleep and deep sleep modes with power options designed to maximize battery life in varying applications

<table>
<thead>
<tr>
<th>Mode</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RUN</strong></td>
<td></td>
</tr>
<tr>
<td>Run</td>
<td>MCU can be run at full speed. Supports Compute Operation clocking option where bus and system clock are disabled for lowest power core processing and energy-saving peripherals with an alternate asynchronous clock source are operational.</td>
</tr>
<tr>
<td>VLP Run (VLPR)</td>
<td>MCU maximum frequency is restricted to 4 MHz core/platform and 1 MHz bus/flash clock. Supports Compute Operation clocking option. LVD protection is off and flash programming is disallowed.</td>
</tr>
<tr>
<td>Wait</td>
<td>Allows all peripherals to function, while CPU goes to sleep reducing power consumption. No Compute Operation clocking option.</td>
</tr>
<tr>
<td>VLP Wait (VLPW)</td>
<td>Similar to VLP Run, with CPU in sleep to further reduce power. No Compute Operation clocking option.</td>
</tr>
<tr>
<td><strong>SLEEP</strong></td>
<td></td>
</tr>
<tr>
<td>Stop</td>
<td>MCU is in static state with LVD protection on. Energy-saving peripherals are operational with Asynchronous DMA (ADMA) feature that can wake-up DMA to perform transfer and return to current mode when complete. AWIC detects wake-up source for CPU. Lowest power mode with option to keep PLL active. Partial stop clocking options for more peripheral functionality available.</td>
</tr>
<tr>
<td>VLP Stop (VLPS)</td>
<td>MCU is in static state with LVD protection off. Energy-saving peripherals are operational with ADMA feature. AWIC detects wake-up source for CPU.</td>
</tr>
<tr>
<td><strong>DEEP SLEEP</strong></td>
<td></td>
</tr>
<tr>
<td>LL Stop (LLS)</td>
<td>MCU is in low leakage state retention power mode. LLWU detects wake-up source for CPU including LPTMR, RTC, TSI, CMP and select pin interrupts. Fast &lt;4.3 us wake-up.</td>
</tr>
<tr>
<td>VLL Stop 3 (VLLS3)</td>
<td>MCU is placed in a low leakage mode powering down most internal logic. All system RAM contents are retained and I/O states held. LLWU controls wake-up source for CPU similar to LLS mode.</td>
</tr>
<tr>
<td>VLL Stop 1 (VLLS1)</td>
<td>Similar to VLLS3 with no RAM or register file retention.</td>
</tr>
<tr>
<td>VLL Stop 0 (VLLS0)</td>
<td>Pin wakeup supported. LPTMR, RTC, TSI and CMP wake-up supported with external clock. No RAM or register file retention. Optional POR brown-out detection circuitry.</td>
</tr>
</tbody>
</table>
Partial Stop (1)

**Wait mode offers limited power savings**
- Only the Cortex-M0+ core is clock gated (~10% of gate count)
- Interrupt controller, crossbar, Flash/SRAM interfaces and bus masters remain functional

**Partial Stop shuts down the core/system clocks**
- Interrupt controller, crossbar, memory interfaces and bus masters are clock gated
- Use the Asynchronous Wakeup Interrupt Controller to detect wakeup event and enable clocks (not supported in Wait mode)
- Peripherals remain functional, same as in Wait mode
- System clock can be gated at root of clock tree
- Can be entered from Run or VLPR modes
Partial Stop (2)

Kinetis MCUs implement staged entry into stop mode as follows:

1. Core/Interrupt Controller enter Stop mode
2. Bus Masters (e.g., DMA) enter Stop mode
   • Can gate system clock
3. Bus Slaves (e.g., Peripherals) enter Stop mode
   • Can gate peripheral clock
4. Clock Generation and PMC enter Stop mode
   • Can disable clock generation

• Partial stop is an option to partially enter Stop mode
  – PSTOP1 implements #1, #2, #3
  – PSTOP2 implements #1, #2
Compute Operation (1)

**Code Execution Mode**
- Reverse of Wait mode
- Core, SRAM and Flash read interfaces remain in Run mode
- Bus Masters and peripherals are placed in Stop mode
- Clock Generation and PMC remain in Run mode
- Can be entered from Run or VLP Run modes

**Peripheral clock gated at root of clock tree**
- Clock gates mode controller and other system modules
- Reset controller supports stop mode reset sources
- Software cannot change clock source or power modes
Compute Operation (2)

Enter/exit Compute Operation via register bit
• Private register only accessible to core
• Must remain accessible during Compute Operation
• Can optionally exit Compute Operation on any interrupt

Peripheral bridge disabled during Compute Operation
• Attempting peripheral access generates bus error
• GPIO (via IOPORT) remains accessible
• Core modules (NVIC, SysTick) also remain accessible

Supports asynchronous operation of peripherals
• Peripherals that are functional in Stop/VLPS modes remain functional in Compute Operation
## Breakthrough Power Efficiency

<table>
<thead>
<tr>
<th>Kinetis Power Modes</th>
<th>Recovery Time</th>
<th>KL26 Measured $I_{dd}$ @ 3 V and 25 C</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Leading Dynamic Power</strong></td>
<td>RUN</td>
<td>-</td>
</tr>
<tr>
<td>Innovative low-power process technology (C90TFS)</td>
<td>VLPR</td>
<td>-</td>
</tr>
<tr>
<td>Low-power-focused platform design</td>
<td>WAIT</td>
<td>1.6 us</td>
</tr>
<tr>
<td>Next-generation Cortex-M0+ core</td>
<td>VLPW</td>
<td>1.6 us</td>
</tr>
<tr>
<td><strong>Asynchronous DMA Wake-Up (ADMA)</strong></td>
<td>STOP</td>
<td>1.3 us</td>
</tr>
<tr>
<td>Energy-saving peripherals are operational with ADMA feature that can wake-up DMA to perform transfer and return to current mode when complete</td>
<td>VLPS</td>
<td>4.2 us</td>
</tr>
<tr>
<td><strong>Low-Leakage Wake-Up Unit</strong></td>
<td>LLS</td>
<td>4.3 us</td>
</tr>
<tr>
<td>Enables complete shut-down of core logic, including AWIC, further reducing leakage currents in all low power modes</td>
<td>VLLS3</td>
<td>39 us</td>
</tr>
<tr>
<td>Supports 8 external input pins and 8 internal modules as wakeup sources, extends the low power wake-up capability of some internal peripherals to all power modes</td>
<td>VLLS1</td>
<td>91 us</td>
</tr>
<tr>
<td>Wake-up inputs are activated in LLS or VLLS modes.</td>
<td>VLLS0</td>
<td>91 us</td>
</tr>
</tbody>
</table>

* Compute Operation enabled: 4.0mA @ 48MHz core / 24MHz bus)
** Compute Operation enabled: 156uA @ 4MHz core / 1MHz bus)

---

**Kinetis Power Modes**

- RUN
- VLPR
- WAIT
- VLPW
- STOP
- VLPS
- LLS
- VLLS3
- VLLS1
- VLLS0

**Recovery Time**

- 1.6 us
- 1.3 us
- 4.3 us
- 39 us
- 91 us

**KL26 Measured $I_{dd}$ @ 3 V and 25 C**

- 79 uA/MHz*
- 39 uA/MHz**
- 2.7 mA @ 48 MHz
- 110 uA @ 4 MHz
- 301 uA
- 2.3 uA
- 1.7 uA
- 1.3 uA
- 700 nA
- 139 nA / 310 nA
# Breakthrough Power Efficiency

<table>
<thead>
<tr>
<th>Feature</th>
<th>Kinetis Power Modes</th>
<th>Recovery Time</th>
<th>KL25 Typical Idd @ 3 V and 25 C</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Leading Dynamic Power</strong></td>
<td>RUN</td>
<td>-</td>
<td>4.1 mA*/ 6.4 mA***</td>
</tr>
<tr>
<td>Innovative low-power process technology (C90TFS)</td>
<td>VLPR</td>
<td>-</td>
<td>188 uA**/ 980 uA***</td>
</tr>
<tr>
<td>Low-power-focused platform design</td>
<td>WAIT</td>
<td>1.6 us</td>
<td>2.9 mA @ 48 MHz</td>
</tr>
<tr>
<td>Next-generation Cortex-M0+ core</td>
<td>VLPW</td>
<td>1.6 us</td>
<td>135 uA @ 4 MHz</td>
</tr>
<tr>
<td><strong>Asynchronous DMA Wake-Up (ADMA)</strong></td>
<td>STOP</td>
<td>4.0 us</td>
<td>345 uA</td>
</tr>
<tr>
<td>Energy-saving peripherals are operational with ADMA feature that can</td>
<td>VLPS</td>
<td>4.0 us</td>
<td>4.4 uA</td>
</tr>
<tr>
<td>wake-up DMA to perform transfer and return to current mode when</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>complete</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Low Leakage Wake-up Unit</strong></td>
<td>LLS</td>
<td>4.0 us</td>
<td>1.9 uA</td>
</tr>
<tr>
<td>Enables complete shut-down of core logic, including AWIC, further</td>
<td>VLLS3</td>
<td>42 us</td>
<td>1.4 uA</td>
</tr>
<tr>
<td>reducing leakage currents in all low power modes</td>
<td>VLLS1</td>
<td>93 us</td>
<td>700 nA</td>
</tr>
<tr>
<td>Supports 8 external input pins and up to 8 internal modules as</td>
<td>VLLS0</td>
<td>95 us</td>
<td>176 nA / 381 nA</td>
</tr>
<tr>
<td>wakeup sources, extends the low power wake-up capability of some</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>internal peripherals to all power modes</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wake-up inputs are activated in LLS or VLLS modes.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Compute Operation enabled: 4.1 mA @ 48MHz core / 24MHz bus*

**Compute Operation enabled: 188uA @ 4MHz core / 800kHz bus**

***Running Coremark algorithm, KEIL 4.54 optimized for speed***
Energy-Saving Peripherals (1)

**Intelligent peripherals increasing time in deep sleep modes with no CPU intervention for increased battery life**

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Low-Power Functionality</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMA</td>
<td>Allows energy-saving peripherals (e.g., ADC, UART and Timer/PWM) to trigger asynchronous DMA request in STOP/VLPS modes to perform DMA transfer and return to current power mode with no CPU intervention</td>
</tr>
<tr>
<td>UART</td>
<td>Supports asynchronous transmit and receive operations to the bus clock supporting communication down to STOP/VLPS modes. Configurable receiver baud rate oversampling ratio from 4x to 32x allowing higher baud rates with lower clock sources.</td>
</tr>
<tr>
<td>SPI</td>
<td>Supports slave mode address match wake-up function and first message capture down to STOP/VLPS modes</td>
</tr>
<tr>
<td>I²C</td>
<td>Supports multiple address match wake-up function down to STOP/VLPS modes</td>
</tr>
<tr>
<td>USB</td>
<td>Supports asynchronous wakeup on resume signaling down to STOP/VLPS</td>
</tr>
<tr>
<td>LPTPM (Timer/PWM)</td>
<td>Supports 16-bit timer input capture, output compare and PWM functions down to STOP/VLPS modes</td>
</tr>
<tr>
<td>LPTMR (Timer/Pulse Counter)</td>
<td>Supports 16-bit timer and pulse counter functions in all power modes</td>
</tr>
<tr>
<td>RTC</td>
<td>Supports 32-bit seconds counter with seconds interrupt and programmable alarm in all power modes with include temperature and voltage compensation</td>
</tr>
</tbody>
</table>
## Energy-Saving Peripherals (2)

Intelligent peripherals increasing time in deep sleep modes with no CPU intervention for increased battery life

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Low-Power Functionality</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Supports single conversions in multiple result registers down to STOP/VLPS modes with</td>
</tr>
<tr>
<td></td>
<td>hardware averaging and automatic compare modes</td>
</tr>
<tr>
<td>CMP (Analog Comparator)</td>
<td>Supports threshold crossing detection in all power modes along with a triggered compare</td>
</tr>
<tr>
<td></td>
<td>mode for lower average power compares</td>
</tr>
<tr>
<td>DAC</td>
<td>Supports static reference in all power modes</td>
</tr>
<tr>
<td>Segment LCD</td>
<td>Supports alternate displays and blink capability in all power modes</td>
</tr>
<tr>
<td>TSI (Capacitive Touch Sense Interface)</td>
<td>Supports wake-on capacitive touch on single channel in all power modes</td>
</tr>
<tr>
<td>LLWU (Low-Leakage Wake-up Unit)</td>
<td>Supports 8 wake-up pins, RESET and NMI wakeup pins, and some energy-saving peripherals</td>
</tr>
<tr>
<td></td>
<td>in LLS and VLLSx modes</td>
</tr>
</tbody>
</table>
Asynchronous DMA Wake-Up

Wake-up from **stop/VLPS** modes to **wait** mode to perform DMA transfer and then re-enter deep sleep mode:

1. Peripheral asserts asynchronous DMA request
2. Exit **stop/VLPS** modes for **wait** mode
3. Peripheral asserts synchronous DMA request
4. Perform DMA transfer
5. Peripheral negates DMA request
6. Re-enter **stop/VLPS** mode
Asynchronous DMA Wake-Up (cont.)

- Supported in Stop and VLPS modes
  - Also supported in Partial Stop modes
  - Also supported in Compute Operation
  - Enabled in DMA Controller per DMA channel (register bit)

- During DMA Wake-up, peripherals are in Wait mode
  - Timers continue incrementing, communication ports may start up
  - Ideally only want peripherals involved in DMA transfer to wake-up

- Keep peripherals disabled during DMA wake-up
  - Software solution is to disable peripherals on Stop entry and enable on Stop exit
  - Hardware solution is to use DOZE bit implemented on many Kinetis peripherals to disable those peripherals in Wait mode
### Asynchronous DMA Wake-Up (cont.)

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Wakeup source</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Conversion complete</td>
</tr>
<tr>
<td>CMP</td>
<td>Compare detected</td>
</tr>
<tr>
<td>I²S</td>
<td>Receive data ready</td>
</tr>
<tr>
<td></td>
<td>Transmit data needed</td>
</tr>
<tr>
<td>LPUART</td>
<td>Receive data ready</td>
</tr>
<tr>
<td></td>
<td>Transmit data needed</td>
</tr>
<tr>
<td>LPTPM</td>
<td>Compare/capture detected</td>
</tr>
<tr>
<td></td>
<td>Counter overflow</td>
</tr>
<tr>
<td>Port Control and Interrupts</td>
<td>External edge detected</td>
</tr>
<tr>
<td>Touch-Sense Interface</td>
<td>End of scan</td>
</tr>
<tr>
<td></td>
<td>Scan out of range</td>
</tr>
</tbody>
</table>
Low-Power UART

UART transmitter/receiver operate asynchronously to bus clock
- Remains fully functional in STOP/VLPS (if clock remains enabled)
- Supports asynchronous interrupt and DMA request
- Supports address match wakeup against two addresses

Configurable receiver oversampling ratio (x4 to x32)
- Input sampled on both clock edges at x4 to x7
- Input data sampled at half the oversampling ratio

Flexible baud rate options
- 4800 bps from 32.768 kHz clock source (OSC or IRCLK)
- Up to 1 Mb/s from 4 MHz clock source (OSC or IRCLK)
- Up to 12 Mb/s from 48 MHz clock source (PLL or FLL)
Low-Power Timer/PWM (TPM) Module

TPM counter operates asynchronous to bus clock
- Remains fully functional in STOP/VLPS (if clock remains enabled)
- Supports input capture, output compare and PWM modes
- Supports asynchronous interrupt and DMA request

All TPM instances can operate from global counter
- Counters not used for global counter can be used separately for pulse accumulation or periodic interrupts or periodic DMA requests

Supports basic trigger generation for triggering ADC
- Can be configured to start incrementing on trigger input, clear counter on trigger input or stop incrementing on overflow
- Eliminates need for PDB module implemented on Kinetis K series MCUs
Other Peripherals

• Analog CMP Low-Power Trigger Mode in all modes
• CMP only enabled periodically to compare analog inputs
• Can use internal 6-bit DAC as comparator reference
• Reduces power consumption while periodically sampling external analog signal
• Triggered by LPTMR

SPI slave mode functional in STOP/VLPS mode
• Generate wake-up after word is received
Kinetis L Series MCUs
Low-power philosophy—“Reducing the gray area under the energy curve.”

Very Low Active and Standby Power Consumption
Ultra-Low Standby Current
Ultra-Low Active Current
(Deep) Sleep Mode
Energy-Saving Peripherals
Reduced Processing Time

**ENERGY SAVINGS**
Kinetis L Series MCUs
Low-power philosophy—“Reducing the gray area under the energy curve.”

- Ultra-Low Active Current
- Ultra-Low Standby Current
- (Deep) Sleep Mode
- Low-Power Boot
- Bit Manipulation Engine
- Optimized Default Setting
- Low Active Current
Kinetis L Series MCUs
Low-power philosophy—“Reducing the gray area under the energy curve.”

- Initialization
- Collect Data
- Compute

- Ultra-Low Active Current
- Ultra-Low Standby Current

- (Deep) Sleep Mode

- RGPIO, 32-bit Register
- Reduced # of Cycles
- Earlier in (Deep) Sleep Mode
- Reduced Frequency
- Reduced Peak Current

ENERGY SAVINGS

- Reduced Number of Cycles
Kinetic L Series MCUs
Low-power philosophy—“Reducing the gray area under the energy curve.”

- Initialization
- Collect Data
- Compute

Ultra-low Active Current
Ultra-low Standby Current
(Deep) Sleep Mode

Multi-choice of Wake-Up Sources (AWIC)
Optimized Wake-Up Sources (LLWU)
Optional Standby/Active Peripherals
State Retention Power Gating
Prolonged (Deep) Sleep Mode
Kinetis L Series MCUs

Low-power philosophy—“Reducing the gray area under the energy curve.”

- Ultra-Low Active Current
- Ultra-Low Standby Current
- (Deep) Sleep Mode
- ENERGY SAVINGS
- Peripherals Optional Active/Standby
- Reduce MHz due to Oversampling (UART)
- Address Match Wake-Up (IIC and SPI)
- Asynchronous/Concurrent DMA Request/Return
- Partial RAM Power (¼ and ¾)
Kineticis L Series MCUs
Low-power philosophy—“Reducing the gray area under the energy curve.”

- Core Optimized for Dynamic Power
- Timer and Pulse Counter in All Modes
- Input Capture, Output Compare and PWM functions in STOP/VLPS
- Crossbar for Concurrent Accesses
- Ultra-Low Standby Current
- Ultra-Low Active Current
- Energy Savings
- (Deep) Sleep Mode

Initialization | Collect Data | Compute
Kinetis L Series MCUs
Low-power philosophy—“Reducing the gray area under the energy curve.”
Kinetic L Series MCUs
Low-power philosophy—"Reducing the gray area under the energy curve."

Ultra-Efficient ARM Cortex-M0+ Core (1.77 CoreMark/MHz)
2x to 40x More Performance Than 8- and 16-bit Architectures
Excellent Code Density vs. 8-bit and 16-bit Architectures
Fast Wake-Up, 2-Stage Pipeline and 15-cycle IRQ Stacking
Reduce RUN Time and increase (Deep) Sleep Time
Kinetis L Series MCUs
Low-power philosophy—“Reducing the gray area under the energy curve.”
Ultra-Low-Power Modes

When should you use each of these modes?

- Each mode has its own advantages and disadvantages and the application drives which mode should be selected.
- Consideration needs to be given to the requirements of the application:
  - Is a fast wake-up time required?
  - Does the RUN current need to be kept below a minimum value?
  - Is flash programming required in the application?
  - What is the active/sleep duty cycle?
  - Are there computational intensive requirements?
  - What peripherals are required to be active?
  - Is accurate timing required in low power modes?
  - What type of wake-up event is required (ext/int)?

- To achieve lowest power, the best mode may not be the one with the absolute lowest IDD.
Ultra-Low-Power Modes

Example
In the case of an application which periodically wakes up for a brief period to perform a task and then enters low power mode, LLS mode may be lower power than even VLLS0.

- The MCU wakes for a short period of time to perform some task.
- It enters low power mode after completing the task.
- If VLLS0 is used, the wake up time is ~100 us with an average current of 4 mA before it can start the task.
- If LLS is used, the wake up time is ~6 us with an average current of ~6 mA before it can start the task.
- VLLS0 wake up draws 4 mA for ~90 us longer than LLS wake-up.
- Delta from LLS (1.76 uA) to VLLS0 (0.4 uA) is 1.36 uA.
- If the additional current drawn during VLLS0 wake-up is compared to the savings of IDD during VLLS0, if you stayed in low-power mode less than ~300 mS, LLS mode actually gives better low power performance.
- This does not take into account the additional delay and current cost of re-initializing the device after VLLS recovery. The “break even” time is typically closer to 500 mS.
Demo
More Information

• Freescale and ROHM Semiconductor partnership achieves the best low power performance and accuracy, with ROHM software development and precision discrete components.

• Ideal for applications that need to measure continuous heart rate monitor through reflective methods (smart watches, ear plugs, etc).

• Demonstration at FTF Americas, launch target date is FTF Japan.