THE NEXT GENERATION OF NON-VOLATILE MEMORY

EVERSPIN TECHNOLOGIES
The MRAM Company™

Freescale Technology Forum - April 2014
GMR effect discovered

Motorola MRAM research delivers first MTJ following two years of R&D

Gersch’s Industry first MRAM (4Mb) commercially available

Everspin Technologies spins off, Raises $20M Series A

Everspin ships 1Mth MRAM, Raises $10.5M Series A1

Everspin releases 16Mb MRAM product

Everspin releases SPI MRAM product family

Everspin ships 4Mth MRAM

Everspin launches industry first ST-MRAM

Everspin ships 1Mth MRAM, Raises $10.5M Series A1

Freescale’s Industry first MRAM (4Mb) commercially available

Everspin announces 256kb – 4Mb MRAM

Everspin ships first embedded MRAM samples

Everspin qualifies 1st eMRAM samples

Everspin ships 2Mth eMRAM

Everspin raises $5M Series A2
MRAM
(Magnetic Random Access Memory)

TECHNOLOGY
Why MRAM?

- Non-Volatile
- Infinite Endurance
- High Speed

- EEPROM
- Flash
- SRAM
- DRAM
- MRAM
Memory Performance

![Memory Performance Chart]

- **Capacity (bits)** vs **Write Cycle Time (ns)**
  - HDD
  - NAND
  - NOR
  - PRAM
  - RRAM
  - FeRAM
  - MRAM
  - DRAM

- **Endurance (cycles)** vs **Write Cycle Time (ns)**
  - HDD
  - NAND
  - NOR
  - RRAM
  - FeRAM
  - PRAM
  - MRAM
  - DRAM

Legend:
- Data Storage
- Working Memory
- Code Storage
MRAM’s Magnetic Tunnel Junction

Magnetic Tunnel Junction

write current

H-field

Free layer
Tunnel barrier
Fixed layer

write current

H-field
Advantages: Eliminates disturb - Large operating window
MRAM (Magnetic Random Access Memory)

- Simple 1 MTJ per transistor
- Magnetic polarization stores data
- Resistance levels represent bit values compared to electron charge levels
- Highly reliable non-volatile memory
- Unlimited endurance & retention
- Low latency enabling instant on/off

Cross-sectional view

Circuit

- Magnetic layer 1 (free layer)
- Tunnel barrier
- Magnetic layer 2 (fixed layer)
- Low resistance
- High resistance
MRAM Write and Read operation

- **WRITE**: Current pulses flow Down Write Line 1 & Write Line 2

- **READ**: Resistance is determined by “Turning on” Pass Transistor to Sense Resistance of MTJ
4Mb Toggle MRAM
Resistance Distributions

- Wide separation of states (“1” and “0” ~ 3k Ohm)
- No image retention
Best in Class Storage & Working Memory

Primary Working Memory
- Ultra-Low Read & Write Latency <50ns
- Unlimited Cycling Endurance >10e15

Persistent Random Access Memory
- Ultra-High Intrinsic Reliability >20yrs@125°C
- Unlimited Data Retention >20yrs@125°C

Storage System Memory
- Robust Power Fail Safe
- No Caps or Batteries
- Instant Power-Off Fast/Safe Shutdown On <2ms

Extreme Environment Memory
- Wide Operating Temperature -40°C – 125°C
- Ultra-Low radiation induced SER <0.1FIT/Mb

Easy BEOL integration with CMOS
Ideal choice for eBuffer/eCache
Endurance
MRAM: Unlimited Read/Write Endurance

- MRAM Endurance Tested to $\sim 6 \times 10^{13}$ Cycles with No Change in Critical Parameters
- Data from >2800 bits from 900 devices
- 8 orders of magnitude more cycles than current Flash technology
- No failure modes observed from cycling
MRAM Data Retention Validation

- **Accelerated data retention testing**
  - Red curve is theoretical model (Arrhenius-Néel) prediction of time to single bit flip vs. temperature for 500-4Mb parts with minimum energy barrier for 20 year retention @ 125 °C
    - $E_b/k_bT = \alpha = 60$

- **Checker board data written in 500 – 4Mb parts**
  - Anneals vs. time performed well past model extremes and data pattern verified

- **No retention error observed in 500 - 4Mb parts**
  - Extreme test times and temperatures indicate retention far exceeds 20 years @ 125 °C requirement

**Note:** ECC off

**Equation:**

$$N = N_0 \left(1 - e^{-\frac{t}{\tau_0 \alpha}}\right)$$

$$\alpha = \frac{E_b}{k_bT}$$

$$\tau_0 = 10^{-9} \text{ s}$$
Products
# Current MRAM Products

## Parallel Asynch SRAM Compatible

<table>
<thead>
<tr>
<th>16-bit I/O</th>
<th>Package Types</th>
</tr>
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<tbody>
<tr>
<td>Part Number</td>
<td>Density</td>
</tr>
<tr>
<td>MR4A16</td>
<td>16 Mb</td>
</tr>
<tr>
<td>MR2A16*</td>
<td>4 Mb</td>
</tr>
<tr>
<td>MR0A16*</td>
<td>1 Mb</td>
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<table>
<thead>
<tr>
<th>8-bit I/O</th>
<th>Package Types</th>
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</thead>
<tbody>
<tr>
<td>Part Number</td>
<td>Density</td>
</tr>
<tr>
<td>MR4A08</td>
<td>16 Mb</td>
</tr>
<tr>
<td>MR2A08*</td>
<td>4 Mb</td>
</tr>
<tr>
<td>MR0A08</td>
<td>1 Mb</td>
</tr>
<tr>
<td>MR256A08</td>
<td>256 Kb</td>
</tr>
<tr>
<td>MR0D08</td>
<td>1 Mb</td>
</tr>
<tr>
<td>MR256D08</td>
<td>256 Kb</td>
</tr>
<tr>
<td>MR0DL08</td>
<td>1 Mb</td>
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<tr>
<td>MR256DL08</td>
<td>256 Kb</td>
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</table>

## Serial SPI Interface

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Density</th>
<th>Configuration</th>
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</thead>
<tbody>
<tr>
<td>MR25H40*</td>
<td>4 Mb</td>
<td>512K x 8</td>
</tr>
<tr>
<td>MR20H40</td>
<td>4 Mb</td>
<td>512K x 8, 50 MHz</td>
</tr>
<tr>
<td>MR25H10*</td>
<td>1 Mb</td>
<td>128K x 8</td>
</tr>
<tr>
<td>MR25H256*</td>
<td>256 Kb</td>
<td>32K x 8</td>
</tr>
<tr>
<td>MR10Q010</td>
<td>1 Mb</td>
<td>Quad SPI, 104 MHz</td>
</tr>
</tbody>
</table>

* Available in AEC-Q100 Automotive Grade
# Persistent SRAM Products

## SRAM and SPI Interfaces

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>Serial SPI Compatible</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>256Kb* 1Mb*</td>
<td>4Mb*</td>
<td>50MHz 4Mb</td>
<td>1Mb Quad</td>
<td>Higher Density Quad SPI</td>
<td></td>
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<tr>
<td><strong>SRAM Compatible SOIC</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>256Kb 1Mb (x8)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SRAM Compatible BGA</strong></td>
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<td></td>
<td></td>
<td></td>
<td>256Kb 1/4Mb 3.3/1.8V (x8)</td>
<td>16 Mb (x16)</td>
<td>16 Mb (x8)</td>
<td>256kb,1Mb 3.3/1.8V V&lt;sub&gt;DD&lt;/sub&gt;=2.7V min</td>
<td>High density SRAM</td>
<td></td>
</tr>
<tr>
<td><strong>SRAM Compatible TSOP2</strong></td>
<td>4Mb (x16)</td>
<td>1Mb (x16)</td>
<td>256Kb 1/4Mb 3.3/1.8V (x8)</td>
<td>256Kb,1Mb 3.3/1.8V (x8)</td>
<td>16 Mb (x16)</td>
<td>16 Mb (x8)</td>
<td>AEC-Q100 4 Mb (x8,x16)</td>
<td>High Density SRAM</td>
<td></td>
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</tr>
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* AEC-Q100

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**Design**  
**Sampling**  
**Production**  

Proprietary & Confidential
Quad SPI and the Flash-less Micro

- Faster than 8-bit parallel
- Low pin count, smaller package than parallel parts
- MCUs appearing with no flash
  - QSPI flash is faster and cheaper
2\textsuperscript{nd} GENERATION MRAM
**MRAM - Technology Comparison**

**Toggle Write**
- Write accomplished by magnetic fields from current passing through bit and word lines.
- In volume production

**Spin-Torque Write**
- Write accomplished by spin polarized current passing through the MTJ.
- In development
Market Expansion: Scaling to Gigabit MRAM

Spin-torque MRAM in the data path as persistent DRAM.

- Inherently more reliable, low latency storage – enabler for NAND SSD
- Buffer/Cache in Drives and RAID systems
- Moving to Storage Server memory
- Ultimately a Storage Class Memory tier

TAM growing from $500M to $26B
APPLICATIONS
MRAM – Diverse & Growing Applications

• Current products
  • Replaces NVSRAM and FRAM with higher performance
  • Asynchronous SRAM and Serial (SPI) Interface

- Routers
- Gaming Systems
- PLC, IA, HMI
- Storage Servers
- Enterprise RAID
- Storage Appliances
- SSD and Hybrids
- Industrial Computing
- Smart Meter/Grid
- Avionics
- Automotive
- Automotive
- Enterprise
- Storage
Memory Consolidation using MRAM

- **Code Space**
  - The unlimited endurance of MRAM enables its use for program storage

- **Working Memory**
  - MRAM is accessed like SRAM
    - No erase cycles
    - No slow write time

- **Non-Volatile data**
  - What non-volatile memory was made for!

- **Code Updates**
  - Download and CRC check code before executing it.
Power Disruption Decision Time

- When a power fail is detected, a system goes into panic mode!
  - Critical data must be saved before power level is too low
- The data backup process when power is failing is the ‘Achilles heel’
- MRAM can save the data very quickly
  - Data gets committed to memory faster
  - MRAM has the fastest write speed of any NV memory
Low Energy Applications

- Energy consumption of the system often dominated by the background energy consumption.
- MRAM can be turned on and off quickly so background energy consumption is zero.
- SPI products have low power features for mobile or battery powered systems.
Everywhere there’s a need for fast write, reliable non-volatile memory...

Automotive Applications for MRAM
The Application
- Point of Sale (POS)
- POS systems are found in cash registers, bill validator, and gaming machines.
- Stored data must be maintained during brownouts, black outs, batch processing, maintenance shutdowns.
- Data is written continuously.

MRAM Improves Data Reliability
- Store transaction data without battery or battery maintenance.
- Infinite endurance write and read.
- Financial data maintained reliably.
Example: RAID

► The Application
- Redundant Array of Inexpensive Disks (RAID 0-7 & Hybrids)
- RAID systems are found in almost all data storage environments
- MRAM stores system information such as restart vectors, controller parameters, system configuration data, other metadata and parity information.
- In case of power failure, the system information needs to be retained and accessed quickly upon restart

► MRAM Improves Data Reliability
- Recommended in RAID controller reference designs
- Application requires high endurance of MRAM
- Fast, unlimited reads and writes
**MRAM Improves Data Reliability**

- Application requires high endurance of MRAM
- Fast, unlimited reads and writes
- Fast 2ms start up

**The Application**

- Storage System Error Logging
- Non-volatile memory stores Error maps used for predicting system failures
- Requires high endurance and power off storage and fast data recovery

**Example: Error Logging**
Example: Reprogramming

The Application: OTAR (Over The Air Re-programming)

- Updating program require two memories
  - Existing program code resides in EEPROM/Flash
  - New/updated program code temporarily placed in SRAM
  - New program must first be verified before Flash/EEPROM can be erased and re-programmed
- Risk involved in power loss while Flashing new program

MRAM eliminates the need for a 2nd memory device

- Due to Byte addressability and non-volatility, software can be updated on a byte by byte basis eliminating the need for either a large or a 2nd memory device
- Software can be made more efficient
  - Saves re-programming time
  - Reduces power
  - Eliminates risk during re-programming
Everspin is the leader in MRAM technology

- Proven track record - manufacturing MRAM since 2006
- Top tier 1 customers
- Deployment in many applications with exemplary quality

Continued MRAM leadership

- Announced the industry’s first ST-MRAM commercial product
- Introduced Ultra high speed Quad SPI family
- Embedded MRAM offering to leverage Spin Torque technology

Scaling to meet future demand

- Expanding Toggle MRAM capacity and sourcing flexibility
- Establishing 300mm ST-MRAM capacity to reduce cost
- Asset light approach in collaboration with partners