Freescale DSC New Product Introduction - **MC56F82xxx**

FTF-IND-F0474

Zhou Xuwei | Application Engineer

**M A Y . 2 0 1 4**
Agenda

- Nevis and Anguilla Silver Introduction
- Core and Key Motor Control Peripherals
- Enablement
- Typical Use Cases
Nevis & Anguilla Silver Introduction

- Nevis: MC56F84xxx
- Anguilla Silver: MC56F82xxx
MC6F82/4xxx
Half the Power, Twice the Performance

100MHz DSP 32-BIT 56800EX Hawk V3 core
- Fastest DSC in its class with 100 MHz of performance
- FIR Filter 6x faster than ARM CortexM3
- The highest number of operations per cycle of any MCU in its class
- Fractional arithmetic
- Nested looping
- Superfast interrupt

The lowest power DSC available on the market
- Less than 0.4mA/Mhz at full speed run
- Concurrent operations offer best-in-class execution times and overall low power run rates.

High Performance DSC Core
- eFlexPWM – Freescale’s most advance timer for Digital Power Conversion with up to 8ch and 312pico-sec resolution, supported by 4 independent time bases, with half cycle reloads for increased flexibility and best in class performance
- NanoEdge placer to implement fractional delays
- Intermodule Cross-Bar directly connecting any input and/or output with flexibility for additional logic functions (AND/OR/XOR/NOR)
- DAC with hardware Waveform generation support
- Very high speed ADCs capture events real time.

High Performance Peripherals
- Advanced Integration & development speed
  - A high level of on-chip integration lowers external Op Amp and capacitor costs.
  - Motor control with integrated Power Factor Correction (PFC) reducing chip count.
  - Motor Control, Power Control, Safety (IEC60730) Libraries, PMBus software stack, PLC software stack.
  - Proven 5 volt tolerant I/O and Peripheral Crossbar enable greater flexibility and system cost reduction.
  - Development tools, including FreeMaster, enable real-time debug monitoring, data visualization, rapid application design, and more.

Lowest Power

Lowest Cost of Design
DSC Roadmap

- **MC56F802x/3x**
  - MC56F803x – 32MHz Hi Res PWM, CAN, ADC, DAC
  - MC56F802x – 32MHz Hi Res PWM, ADC, DAC

- **MC56F800x**
  - MC56F800x – 32MHz Hi Res PWM

- **MC56F824x/5x**
  - MC56F825x – 60MHz 64K Flash Ultra-Hi Res PWM, UHS ADC
  - MC56F824x – 60MHz 48K Flash Ultra-Hi Res PWM, UHS ADC

- **MC56F84xxx**
  - 56F8441 – 100MHz 32-bit Core 256K Flash DMA, UHS ADC, Ultra-Hi Res PWM
  - 56F8432/1 – 100MHz 32-bit Core 128K Flash DMA, UHS ADC, Ultra-Hi Res PWM
  - 56F8422/1 – 100MHz 32-bit Core 64K Flash DMA, UHS ADC, Ultra-Hi Res PWM

- **Nevis**
  - 2012
  - 120MHz 32-bit Core 256K Flash FPU

- **MC56F85xx**

- **MC56F82xxx**
  - 50/100MHz 64K Flash Ultra-Hi Res PWM UHS ADC

- **MC56F80xx**
  - Low power
  - Small Flash Blocks
  - Hi Res PWM

- **Ang. Blue**
- **Ang. White**
- **Ang. Black**
- **Ang. Silver**
- **Ang. Nano**
Freescale DSC Family Compatibility

- **NVM KB**
  - 256
  - 128
  - 64
  - 48
  - 32

- **Package**
  - 44LQFP
  - 48LQFP
  - 64LQFP
  - 80 / 100LQFP

- **Available**
- **Announced**
- **Planned**

- **PIN COMPATIBLE**
- **56F8255**
- **56F8245**
- **56F82xxx**
- **56F82xxx**
- **56F8246**
- **56F8247**
- **56F82xxx**
- **56F82xxx**
- **56F84xxx**
- **56F84xxx**
- **56F84xxx**
- **56F84xxx**
MC56F84xxx Features

- 100 MHz/100MIPS 56800 V3 Core
  - Harvard architecture
  - 32 x 32bit MAC and 32bit arithmetic operation
- 2.7-3.6V Operation
- 256kB Program/Data FLASH
- 32kB Data Flash with up to 2kB of eEE
- 32kB Data/Program RAM
- Resource Protection Unit
- 3 HS-QSCI (8MBS), 3xQSPI, 2xIIC/SMBus, 1xFlexCAN
- Multi-purpose timers
  - 2 Periodic Timers with Real Time Interrupt Generation
  - 2 Programmable Delay Blocks
  - 8Ch multifunction timers
- 8ch High Resolution PWM Channels
  - 312ps PWM and PFM resolution
  - 8ch PWM Channels with Input Capture
- 8ch x 2 12-bit ADC converter with built-in PGA
  - 300ns/3.33Mmps conversion time with 12bit resolution
- 8ch 16bit SAR ADC with built-in temperature sensor and band gap.
  - 2us conversion time.
- 4 Analog Comparators
- 1 Quadrature Decoder
- 1ch 12bit DAC with external outputs + 4ch 6bit DAC
- DMA controller
- Inter-Module Crossbar
- On-chip voltage regulator (Single 3.3V Power Supply)
- System Integration: Internal relaxation oscillator, PLL, COP, 32kHz, EWM, auxiliary Internal clock, low voltage detect, EZPort
- 5V tolerant I/O
- Temperature Range: -40°C to +105°C

48 LQFP, 64 LQFP, 80LQFP, 100LQFP
# 56F84000 Series Feature Summary

## MC56F84xxx

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Fully Featured</th>
<th>Digital Control</th>
<th>Digital Control</th>
<th>Dual Motor</th>
<th>Single Motor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core MHz</td>
<td>789</td>
<td>786</td>
<td>769</td>
<td>766</td>
<td>763</td>
</tr>
<tr>
<td>Flash Mem (kB)</td>
<td>256</td>
<td>256</td>
<td>128</td>
<td>128</td>
<td>128</td>
</tr>
<tr>
<td>SRAM Mem (kB)</td>
<td>32</td>
<td>32</td>
<td>24</td>
<td>24</td>
<td>24</td>
</tr>
<tr>
<td>Data Flash / EE Mem (kB)</td>
<td>32/2</td>
<td>32/2</td>
<td>32/2</td>
<td>32/2</td>
<td>32/2</td>
</tr>
<tr>
<td>Cyc ADC Chn</td>
<td>2x8</td>
<td>2x8</td>
<td>2x8</td>
<td>2x8</td>
<td>2x8</td>
</tr>
<tr>
<td>SAR ADC Chn</td>
<td>1x16</td>
<td>1x16</td>
<td>1x16</td>
<td>1x16</td>
<td>1x16</td>
</tr>
<tr>
<td>PWM uE Chn</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>PWM std Chn</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>DAC</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Quad Decoder</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>DMA</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>CMP</td>
<td>4</td>
<td>4</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>QSCI</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>QSPI</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>I2C</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>FlexCAN</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Package</td>
<td>100</td>
<td>80</td>
<td>100</td>
<td>80</td>
<td>80</td>
</tr>
</tbody>
</table>

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*External Use | 7*
### MC56F82xxx – Anguilla Silver

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>56800EX V3 Core</strong> @ 50MHz (100MHz from RAM)</td>
<td>2.7-3.6V Operation</td>
</tr>
<tr>
<td><strong>Up to 64KB Program FLASH ,with Flash Security</strong></td>
<td>Up to 6KB Program/Data RAM</td>
</tr>
<tr>
<td><strong>Memory Resource Protection Unit</strong></td>
<td>Up to 100 MHz Peripherals – Timers and SCIs</td>
</tr>
<tr>
<td><strong>Eight Channel Nano Edge PWM (512ps resolution)</strong></td>
<td>- Up to four programmable fault protection input</td>
</tr>
<tr>
<td></td>
<td>- Dead-time insertion</td>
</tr>
<tr>
<td></td>
<td>- Input Capture function</td>
</tr>
<tr>
<td><strong>2 x12-bit ADCs with total 16 Inputs &amp; PGAs 1x, 2x, 4x</strong></td>
<td>- 800ns conversion rate</td>
</tr>
<tr>
<td></td>
<td>- Band-gap reference</td>
</tr>
<tr>
<td><strong>Four channel DMA controller</strong></td>
<td><strong>Inter Module cross-bar</strong></td>
</tr>
<tr>
<td><strong>4 x Comparators with a 6bit Voltage reference</strong></td>
<td><strong>CRC Generator</strong></td>
</tr>
<tr>
<td></td>
<td>- 2 x Windowed Watchdog</td>
</tr>
<tr>
<td></td>
<td>- External Watchdog Monitor</td>
</tr>
<tr>
<td><strong>4 x 16-bit Enhanced Multifunction Programmable Timers</strong></td>
<td>- 2 x 12b DAC</td>
</tr>
<tr>
<td></td>
<td>- 2 x High Speed SCI</td>
</tr>
<tr>
<td></td>
<td>- 2 x SPI</td>
</tr>
<tr>
<td><strong>1x I²C/SMbus Communications Interface</strong></td>
<td><strong>Software Programmable Phase Locked Loop</strong></td>
</tr>
<tr>
<td><strong>Multiple Clock sources</strong></td>
<td>- External Crystal/Resonator Oscillator</td>
</tr>
<tr>
<td></td>
<td>- 8MHz/200KHz Tunable Internal Relaxation Oscillator</td>
</tr>
<tr>
<td></td>
<td><strong>200kHz Internal RC relaxation Oscillator</strong></td>
</tr>
<tr>
<td><strong>5v Tolerant IO</strong></td>
<td><strong>Error code correction</strong></td>
</tr>
<tr>
<td><strong>Industrial temperature:-40C to 105C @ 50MHz</strong></td>
<td></td>
</tr>
</tbody>
</table>

**Packages will be pin compatible with the MC56F824x/5x and MC56F84xx**

### Breakthrough Features:
- High speed ADC @ 800ns conversion time
- Nano Edge PWM @ 512ps Resolution
- Inter-module Cross bar
- DMA
- Memory Resource Protection Unit
## 56F82xxx Series Feature Summary

<table>
<thead>
<tr>
<th>Part Number</th>
<th>MC56F82</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>748VL H</td>
</tr>
<tr>
<td>Core frequency (MHz)</td>
<td>100/50</td>
</tr>
<tr>
<td>Flash memory (KB)</td>
<td>64</td>
</tr>
<tr>
<td>RAM (KB)</td>
<td>8</td>
</tr>
<tr>
<td>12-bit Cyclic ADC channels</td>
<td>2x8</td>
</tr>
<tr>
<td>PWMA with input capture:</td>
<td></td>
</tr>
<tr>
<td>High-resolution channels</td>
<td>1x8</td>
</tr>
<tr>
<td>Standard channels</td>
<td>0</td>
</tr>
<tr>
<td>12-bit DAC</td>
<td>2</td>
</tr>
<tr>
<td>DMA</td>
<td>Yes</td>
</tr>
<tr>
<td>CMP</td>
<td>4</td>
</tr>
<tr>
<td>QSCI</td>
<td>2</td>
</tr>
<tr>
<td>QSPI</td>
<td>2</td>
</tr>
<tr>
<td>I2C/SMBus</td>
<td>1</td>
</tr>
<tr>
<td>MSCAN</td>
<td>1</td>
</tr>
<tr>
<td>GPIO</td>
<td>54</td>
</tr>
<tr>
<td>LQFP package pin count</td>
<td>64 LQFP</td>
</tr>
</tbody>
</table>
**Freescale DSC Performance vs. Competitors**

**Freescale Value Proposition**
- Dynamic Performance - The greatest number of operations per cycle of any MCU in its class

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Freescale DSC</th>
<th>TI Piccolo</th>
<th>Microchip dsPIC</th>
<th>STMicro STM32</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core / Speed</td>
<td>56800EX</td>
<td>C28x</td>
<td>dsPIC33F/E</td>
<td>CortexM4</td>
</tr>
<tr>
<td></td>
<td>Up to 100MHz</td>
<td>Up to 80MHz</td>
<td>Up to 70MHz</td>
<td>Up to 168MHz</td>
</tr>
<tr>
<td>Data Types</td>
<td>Integer &amp; Fractional</td>
<td>Integer</td>
<td>Integer &amp; Fractional</td>
<td>Integer</td>
</tr>
<tr>
<td>Buses</td>
<td>3 address / 4 data</td>
<td>3 address / 3 data</td>
<td>3 address / 4 data</td>
<td>3 (I-bus/D-bus/S-bus)</td>
</tr>
<tr>
<td>Memory Maps</td>
<td>Separate program &amp; data</td>
<td>Unified program and data</td>
<td>Separate program &amp; data</td>
<td>Unified program and data</td>
</tr>
<tr>
<td>Pipeline Depth</td>
<td>8</td>
<td>8</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Math Operations per Instruction</td>
<td>6</td>
<td>4</td>
<td>6</td>
<td>5</td>
</tr>
<tr>
<td>Accumulators</td>
<td>4 ACCs (36 bits)</td>
<td>1 ACC (32 bits)</td>
<td>2 ACCs (40 bits)</td>
<td>N/A (0-8 reg)</td>
</tr>
<tr>
<td>DMA</td>
<td>Up to 4-ch</td>
<td>Up to 6-ch</td>
<td>Up to 15-ch</td>
<td>Up to 16-ch</td>
</tr>
<tr>
<td>Interrupt Controller</td>
<td>Hardware Priority Fast ISR</td>
<td>No Hardware Priority</td>
<td>Hardware Priority</td>
<td>Hardware Priority</td>
</tr>
<tr>
<td>Architecture Advantages</td>
<td>Intermodule Crossbar Switch, Nested Interrupts (no need for CLA)</td>
<td>CLA, VCU, FPU</td>
<td>Peripheral Pin Select (PPS) for pin function remap</td>
<td>ART Accelerator, FPU, Multi-level AHB bus matrix</td>
</tr>
<tr>
<td>Flash</td>
<td>Up to 288KB TFS 90nm</td>
<td>Up to 256KB + 2KB OTP Requires Paging</td>
<td>Up to 536KB</td>
<td>Up to 1MB +512B OTP Multiple Incompatible Technology Nodes</td>
</tr>
<tr>
<td>Cache</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes (ART Accelerator)</td>
</tr>
<tr>
<td>RAM</td>
<td>Dual Port</td>
<td>Single Port</td>
<td>Single Port</td>
<td>Single Port</td>
</tr>
<tr>
<td>EEPROM</td>
<td>Yes, up to 2KB</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Memory Corruption Protection</td>
<td>Yes – memory resource protection</td>
<td>No</td>
<td>No</td>
<td>Yes – memory protection unit</td>
</tr>
</tbody>
</table>
Freescale DSC Measure & Control vs. Competitors

**Freescale Value Proposition**
- High Performance on-chip Peripherals - A high level of on-chip integration to reduce software overhead and total BOM cost.

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Freescale DSC</th>
<th>TI Piccolo</th>
<th>Microchip dsPIC</th>
<th>STMicro STM32</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Analog CMP response time</strong></td>
<td>25ns</td>
<td>30ns</td>
<td>20ns</td>
<td>None</td>
</tr>
<tr>
<td><strong>CMP</strong></td>
<td>4 w/6-bit DAC</td>
<td>3</td>
<td>4</td>
<td>None</td>
</tr>
<tr>
<td><strong>DAC</strong></td>
<td>Up to 2x12-bit w/ Hardware Slope Compensation</td>
<td>3x10-bit</td>
<td>4x10-bit</td>
<td>2x12-bit</td>
</tr>
<tr>
<td><strong>ADC Blocks</strong></td>
<td>2 (w/ one S&amp;H for each ADC) 1 w/ High Input Impedance (enabling lower cost ext. Op Amp &amp; Cap)</td>
<td>1 (w/dual S&amp;H)</td>
<td>2 (w/up to five S&amp;H for one SAR, one S&amp;H for another SAR)</td>
<td>3 (w/ dual S&amp;H for regular group and injected group in each ADC)</td>
</tr>
<tr>
<td><strong>ADC conversion</strong></td>
<td>Up to 300ns @ 12-bit</td>
<td>Up to 217ns @ 12-bit</td>
<td>Up to 500ns @ 10-bit 2,000ns @ 12-bit</td>
<td>417ns @ 12-bit</td>
</tr>
<tr>
<td><strong>ADC channels</strong></td>
<td>16-ch 12-bit 8ch 16-bit</td>
<td>16-ch 12-bit</td>
<td>32-ch 10/-12-bit</td>
<td>24-ch 12-bit</td>
</tr>
<tr>
<td><strong>Temp Sensor</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>PWM</strong></td>
<td>Total 16-ch / 8-ch with 312.5ps resolution</td>
<td>Total 19-ch / 8-ch with 150ps resolution</td>
<td>Total 18-ch with1.04ns resolution</td>
<td>Total 14-ch with 5.95ns resolution</td>
</tr>
<tr>
<td><strong>PWM Features</strong></td>
<td>Multiple time base, enhanced capture functionality Edge locked loop for stable PWM edge control Fractional clock calculation and tracking, effectively reducing the software workloads. submodule to submodule synchronization has no delay</td>
<td>Multiple time base, PWM chopper Open loop delay, no stable edge over temp Fractional clock calculation is handled manually</td>
<td>Multiple time base, capture and chopper functionality</td>
<td>Capture functionality</td>
</tr>
<tr>
<td><strong>Timer</strong></td>
<td>8-ch 16-bit QTImeR / 2-ch 16-bit PIT / 2-ch 16-bit PDB</td>
<td>3-ch 32-bit CPU timer</td>
<td>9-ch 16-bit timer / 1-ch RTCC</td>
<td>12-ch 16-bit Timer / 1-ch RTC</td>
</tr>
<tr>
<td><strong>I/O</strong></td>
<td>5V Tolerance on all I/O</td>
<td>Only 3v</td>
<td>5V Tolerance on digital I/O</td>
<td>5V Tolerance on all I/O</td>
</tr>
</tbody>
</table>
Core and Key motor control peripherals

- 56800 EX Hawk V3
- eFlexPWM
- ADC
- Crossbar
### Core
- **56800EX**
  - Up to 100 MHz
- Instruction Shadow Registers
- Fast Nested Interrupts
- 32-bit Instruction Set
- 32b Instr Cache & Prefetch
- eOnCE Interface

### System
- Memory Resource Protection
- 4-ch DMA
- InterModule Crossbar
- Vref
- Quadrature Decoder

### Memories
- Program Flash Up to 256KB
- SRAM 32KB
- FlexMemory 32KB Flash or 2KB EEPROM

### Clocks
- Phase Locked Loop
- Crystal OSC
- 8MHz OSC
- 200KHz OSC

### Security & Integrity
- Cyclic Redundancy Check (CRC)
- Dual Watchdog w/ ext source

### Timers
- eFlexPWM
  - Deadtime
  - Input Capture
  - Fault detect
- NanoEdge Placer
- 4Ch 16b Timer
- 2 x PITs

### Analog
- 8ch 12bit ADC @800ns with PGA
- 12bit DAC
- Band-Gap Ref & Temp Sensor
- 4 x ACMP w/ 6b DAC

### Communication Interfaces
- 2x I²C/SMBus
- 3xUART
- 3xSPI
- CAN
56800EX Hawk V3 Core

Core
- 56800EX
  - Up to 100 MHz
- Instruction Shadow Registers
- Fast Nested Interrupts
- 32-bit Instruction Set
- 32-bit Instruction Cache & Prefetch
- eOnCE Interface

System
- Memory Resource Protection
- 4-ch DMA
- InterModule Crossbar
- Vref
- Quadrature Decoder

Memories
- Program Flash
  - Up to 256KB
- SRAM
  - 32KB
- FlexMemory
  - 32KB Flash
  - or 2KB EEPROM

Clocks
- Phase Locked Loop
- Crystal OSC
- 8MHz OSC
- 200KHz OSC

Security & Integrity
- Cyclic Redundancy Check (CRC)
- Dual Watchdog w/ ext source

Timers
- eFlexPWM
  - Deadtime
  - Input Capture
  - Fault detect
- NanoEdge Placer
- 4Ch 16b Timer
- 2 x PITs

Analog
- 8-ch 12-bit ADC @800ns with PGA
- Band-Gap Ref & Temp Sensor
- 12-bit DAC
- 4 x ACMP w/ 6b DAC

Communication Interfaces
- 2x I²C/SMBus
- 3xUART
- 3xSPI
- CAN

Analog
- 12-bit DAC
- Quadrature Decoder

Analog
- eFlexPWM
  - Deadtime
  - Input Capture
  - Fault detect
- NanoEdge Placer
- 4Ch 16b Timer
- 2 x PITs

Communication Interfaces
- 2x I²C/SMBus
- 3xUART
- 3xSPI
- CAN

Analog
- 12-bit DAC
- Quadrature Decoder

Communication Interfaces
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Analog
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Communication Interfaces
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Communication Interfaces
- 2x I²C/SMBus
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Analog
- 12-bit DAC
- Quadrature Decoder

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- 3xUART
- 3xSPI
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Mapping the Architecture to DSP Algorithms

Common Operation in DSP

<table>
<thead>
<tr>
<th>MAC X0, Y0, A</th>
<th>X:( R4)+, Y1</th>
<th>X:( R3)+, C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arithmetic Op</td>
<td>1st Read</td>
<td>2nd Read</td>
</tr>
</tbody>
</table>

Operations Performed:
- Multiply-Accumulate
- 3 Memory Accesses
- 2 Address Additions

Instruction Fetch:
- PAB - 21 bits
- PDB - 16 bits

1st Data Access:
- XAB1 - 24 bits
- CDBR - 32 bits

2nd Data Access:
- XAB2 - 24 bits
- XDB2 - 16 bits

Program Memory

Data Memory

IP-Bus Interface

External Bus Interface

Operations Performed:
- Multiply-Accumulate
- 3 Memory Accesses
- 2 Address Additions

Instruction Fetch:
- PAB - 21 bits
- PDB - 16 bits

1st Data Access:
- XAB1 - 24 bits
- CDBR - 32 bits

2nd Data Access:
- XAB2 - 24 bits
- XDB2 - 16 bits
DSP 56800E Version 3 Core Improvement
(the differences between V2 core and V3 core)

New Instructions

• 32 x 32 -> 32/64 Multiply and MAC Instructions
  ✓ IMAC32 - Integer Multiply-Accumulate 32 bits x 32 bits -> 32 bits
  ✓ IMPY32 - Integer Multiply 32 bits x 32 bits -> 32 bits
  ✓ IMPY64 - Integer Multiply 32 bits x 32 bits -> 64 bits
  ✓ IMPY64UU - Unsigned Integer Multiply 32 bits x 32 bits -> 64 bits
  ✓ MAC32 - Fractional Multiply-Accumulate 32 bits x 32 bits -> 32 bits
  ✓ MPY32 - Fractional Multiply 32 bits x 32 bits -> 32 bits
  ✓ MPY64 - Fractional Multiply 32 bits x 32 bits -> 64 bits

• Multi-Bit Clear-Set instruction to improve flexibility of peripheral register handling – BFSC (test bitfield and set/clear).

Other Features

• Bit Reversed Address Mode For FFT algorithms.
• Swap all address generation Unit Registers with Shadowed registers to reduce Interrupt context switch latency.
Enhanced Flex Pulse Width Modulator (eFlexPWM)

- **Four independent sub-modules** with own time base, two PWM outputs + 1 auxiliary PWM input/output
- 16 bits resolution for center, edge aligned, and asymmetrical PWMs
- For enhanced resolution of the PWM period and edge placement
- Complementary pairs or independent operation
- Independent control of both edges of each PWM output
- **Synchronization** to external hardware or other PWM sub-modules
- Double buffered PWM registers
- Integral reload rates from 1 to 16 include half cycle reload
- Half cycle reload capability
- **Multiple output trigger events per PWM cycle**
- Support for double switching PWM outputs
- **Fault inputs** can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Individual software control for each PWM output
- Software control, and swap features via FORCE_OUT event
- Compare/capture functions for unused PWM channels
- Enhanced dual edge capture functionality
eFlexPWM – 56F824x/5x – Block Diagram – Sub-ModuleX

PWM generation – block diagram

- Clock
- PWM Generator
  - PWM pattern – top transistor
  - PWM pattern – bottom transistor
- Force Out Logic
  - PWM gen - PWM23
  - Software - OUT23
  - External signal - EXTA
  - PWM gen – PWM45
  - Software – OUT45
  - External signal – EXTB
- Deadtime Insertion
  - Independent/Complementary operation
  - Deadtime insertion
  - PWM23
  - PWM45
- Output Logic
  - Mask control
  - Polarity control
  - PWM output enable/disable
  - Fault control
- Fractional Delay
  - Fractional delay 23 – 5-bit
  - Fractional delay 45 – 5-bit
  - PWM23
  - PWM45
- PWMA output
- PWMB output
eFlexPWM - Sub-Module Detail
eFlexPWM – Edge Aligned PWM Generation

VAL1 ($0100)

VAL5 ($0000)

VAL3

INIT ($FF00)

VAL2, VAL4 = $FF00

CH0<sub>b</sub>

CH0<sub>a</sub>

- All PWM-on values are set to the init value, and never changed again. Positive PWM-off values generate pulse widths above 50% duty cycle. Negative PWM-off values generate pulse widths below 50% duty cycle. This works well for bipolar waveform generation.
eFlexPWM – Center Aligned PWM Generation

When the Init value is the signed negative of the Modulus value, the PWM module works in signed mode. Center-aligned operation is achieved when the turn-on and turn-off values are the same number, but just different signs.
eFlexPWM – Complementary and Deadtime Logic

Diagram showing the eFlexPWM circuit with components labeled as follows:

- PWM23
- DBLPWM
- DBLEN
- IPOL
- DTCNT0
- DTCNT1
- rising edge detect
- falling edge detect
- start
- down counter
- zero
- PWM45
- INDEP

Connections and logic flow are indicated with arrows and gates.
eFlexPWM – Fractional Delay and Output Logic
Challenge of Controlling Resonate Converters

• Challenge:
  - Switched Mode Power Supplies use PWM switching frequencies from 100KHz up to 1Mhz
  - Control loops require very high resolution of PWM in range of nsec (standard PWM @100MHz gives 10nsec resol.)
  - Generation of both high resolution duty cycle and high resolution frequency needed

• Solution on eFlexPWM:
  - High speed digital PWM plus Analog edge delay
  - Fractional delay block increases the resolution 32x (100MHz -> 3.2GHz)
  - For high resolution frequency special H/W circuit automatically increments the PWM period by repositioning edges

High resolution PWM frequency requires small incremental adjustment of both PWM edges
eFlexPWM – High Resolution Duty Cycle Generation

• PWM resolution is given by input clock of PWM module

• The PWM resolution can be enhanced by analog delay circuit, which can place edge between two edges, derived from input clock

• Example:
  - Consider 2-bit analog delay block
  - Let’s generate PWM signal with MODULO=4:0, DUTY_CYCLE=2:3 (68.75 %)
eFlexPWM – High Resolution Duty Cycle Generation

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- Example:
  - Consider 2-bit analog delay block
  - Let’s generate PWM signal with MODULO=4:0, DUTY_CYCLE=2:3 (68.75 %)
eFlexPWM – High Resolution Duty Cycle Generation

- At high resolution duty cycle generation
  - The leading edge is usually aligned with digital clock
  - The falling edge is generated by delay block
  - The analog delay is constant every PWM period

![Diagram showing PWM output with and without delay block]
eFlexPWM – High Resolution Freq. Generation

• Example:
  - Consider 2-bit analog delay block
  - Let’s generate PWM signal with MODULO=4:2, DUTY_CYCLE=2:1 (50 %)

• At high resolution frequency generation
  - Both edges are generated by delay block
  - The analog delay is changing edge by edge every PWM period
  - The analog delay must be calculated every edge or requires hardware support
eFlexPWM

• More information : AN4746 (High-Resolution PWM Generation Using MC56F82xx, MC56F84xxx, MC56F823xx, and MC56F827xx DSC Families)
### Core
- **56800EX**
  - Up to 100 MHz
- Instruction Shadow Registers
- Fast Nested Interrupts
- 32b Instruction Set
- Parallel Instruction Moves
- 32b Instr Cache & Prefetch
- eOnCE Interface

### System
- Memory Resource Protection
- 4-ch DMA
- InterModule Crossbar
- Vref
- Quadrature Decoder

### Memories
- Program Flash Up to 256KB
- SRAM 32KB
- FlexMemory 32KB Flash or 2KB EEPROM

### Clocks
- Phase Locked Loop
- Crystal OSC
- 8MHz OSC
- 200KHz OSC

### Security & Integrity
- Cyclic Redundancy Check (CRC)
- Dual Watchdog w/ ext source

### Timers
- eFlexPWM
  - Deadtime
  - Input Capture Fault detect
- NanoEdge Placer
- 8ch 12bit ADC @800ns with PGA
- 4Ch 16b Timer
- 2 x PITs

### Analog
- 12bit DAC
- Band-Gap Ref & Temp Sensor
- 4 x ACMP w/ 6b DAC
- 8ch 12bit ADC @800ns with PGA

### Communication Interfaces
- 2x I²C/SMBus
- 3xUART
- 3xSPI
- CAN
A/D Converter

- 12-bit resolution
- Single conversion time of 8.5 ADC clock cycles (8.5 × 50 ns = 450 ns)
- Additional conversion time of 6 ADC clock cycles (6 × 50 ns = 300 ns)
- ADC to PWM synchronization
- Scans and stores up to eight measurements each on two ADC converters
- Multi-triggering support
- Gains the input signal by x1, x2, or x4
- Optional sample correction by subtracting a pre-programmed offset value
ADC Channel Scan Modes

Once
The ADC starts to sample just one time whether you use the START bit or by a sync pulse. This mode must be re-armed by writing to the ADCR1 register again if you want to go capture another scan.

Triggered
Sampling begins with every recognized START command or sync pulse.

Loop
The ADC continuously take samples as long as power is on and the STOP bit has not been set.

Sequential Mode
Sequential will sample SampleN one after another. Channel ANAx are sampled by ADCA and Channel ANBx are sampled by ADCB.

Parallel Mode
Simultaneous: Parallel can sample SampleN from Group1 and SampleN from Group2 at the same time.

Independent:: ADCA and ADCB can operate independently. At end of scan of each ADC, they generate separate interrupt request.
Why ADC to PWM Synchronization is needed?

- ADC Sampling helps to filter the measured current - antialiasing

![Diagram showing ADC to PWM synchronization]

- ADC trigger Signal
- Average Current
  - Sampled Current
  - Inductor Current
- PWM 0
- Data Processing and New PWM Parameters Calculation
Current Sensing with Shunt Resistors

- Shunt resistors voltage drop measured
- Dual-sampling required

![Diagram of current sensing with shunt resistors]

- PWM At
- PWM Bt
- PWM Ct
- PWM Ab
- PWM Bb
- PWM Cb

3-ph AC Induction Motor
3-ph PM Synchronous Motor

ADC Sampling Point

Real feedback signal at ADC pin

Rising edge is shifted by DT

Mid point shifts

Complementary pair with dead time inserted (signals at pins)
# Crossbar

## Core
- 56800EX
- Up to 100 MHz
- Instruction Shadow Registers
- Fast Nested Interrupts
- 32-bit Instruction Set
- Parallel Instruction Moves
- 32-bit Instr Cache & Prefetch
- eOnCE Interface

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- FlexMemory 32KB Flash or 2KB EEPROM

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- Phase Locked Loop
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- 8MHz OSC
- 200KHz OSC

## Security & Integrity
- Cyclic Redundancy Check (CRC)
- Dual Watchdog w/ ext source

## Timers
- eFlexPWM
- 8ch 12bit ADC @800ns with PGA
- 4-bit DAC
- NanoEdge Placer
- 4-ch 16-b Timer
- 2 x PITs

## Analog
- 8ch 12bit ADC @800ns with PGA
- 12-bit DAC
- Band-Gap Ref & Temp Sensor
- 4 x ACMP w/ 6-bit DAC

## Communication Interfaces
- 2x I²C/SMBus
- 3x UART
- 3xSPI
- CAN
Crossbar Switch - MC56F824x/5x

- Flexible signal interconnection among peripherals
- Connects any of 22 signals on left side to the output on right side (multiplexer)
- Total 30 multiplexers
- All multiplexers share the same set of 22 signals
- Increase flexibility of peripheral configuration according to user needs
Crossbar Inter-module Connection - MC56F84xxx

Crossbar B

AND-OR-INV Logic
AND-OR-INV Logic
AND-OR-INT Logic
AND-OR-INV Logic

Crossbar A

DMA Req
INT
n
n
n
n
n
n
n
n
n6
eFlexPWM
HS-CMP
Timer
Q_Decoder
I/O
PDB
Enablement

- Motor control hardware kits
- FreeMASTER
- QuickStart
- Embedded software libraries
- IEC60730 libraries
## Tools and Software

<table>
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<tr>
<th>Hardware Kits</th>
<th>FreeMASTER</th>
<th>CodeWarrior</th>
<th>Run Time Software</th>
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</thead>
<tbody>
<tr>
<td>- Tower</td>
<td>Real-Time Debug, Monitoring and Visualization GUI development Tool</td>
<td>Comprehensive IDE that provides a highly visual, automated framework to accelerate development of some of the most complex embedded applications</td>
<td>Digital Power Library Motor Control Library Filter Library Safety Library PMBUS Stack CAN Stack &amp; more ........</td>
</tr>
<tr>
<td>Development Kit</td>
<td>TWR-56F8400</td>
<td>- High Voltage and Low Voltage Motor Control &amp; Power Conversion Boards</td>
<td></td>
</tr>
</tbody>
</table>

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<thead>
<tr>
<th>QEDesign Lite</th>
<th>Processor Expert &amp; QuickStart Init Tools</th>
<th>Reference Designs</th>
<th>MCAT</th>
</tr>
</thead>
</table>
| Complimentary graphical filtering tool used to auto-generate coefficients that drop into any project. Ideal for designing any type of filter | Rapid Init Code Generation combines easy-to-use component-based application creation with an expert knowledge system Quick Start Easy-to-use SW Development Environment for includes initialization and Run-Time drivers | Complimentary code and schematics for :  
  - various motor control  
  - LLC resonant converter  
  - Solar power conversion  
  - Wireless Charging  
  - Lighting | • real-time tuning and debugging of the motor control applications  
  • helping in connecting and tuning new electric drive |
Motor Control
Hardware Kits
Tower Low Voltage Power Control Board

- Tower system module for BLDC / PMSM control
- Support most of current and new TWR MCU modules
- Launched kit includes power supply and BLDC motor with application examples using K40 and MC56F825x devices

- Features:
  - Power supply voltage input 24VDC
  - Output current up to 8 Amps
  - Power supply reverse polarity protection circuitry
  - 3-phase bridge inverter (6-MOSFET’s) with over-current and under-voltage protection
  - 3-phase and d.c. bus-current-sensing shunts
  - DC bus-voltage and 3-phase back-EMF voltage sensing
  - Low-voltage on-board power supplies
  - Encoder/Hall sensor sensing circuitry

Product Page at Freescale.com: TWR-MC-LV3PH
3-ph BLDC/PMSM High Voltage MC Drive

- **Main board + MCU daughter cards**
- **Available MCU cards:**
  - MC9S08MP16
  - MC56F8006 / MC56F8013 / MC56F8023
  - MC56F8257
  - MC56F82xxx
  - K40X256

- **Board Features:**
  - Input Voltage 115-230Vac, 50/60Hz / Output Power 1kW
  - 3-phase IGBT inverter bridge with over-current protection
  - Interleave PFC (coming in Rev2)
  - 3-phase motor current and BEMF sensing
  - DC-Bus current and voltage sensing
  - Isolated SCI / USB interface
  - User LED’s
  - Encoder / Hall Sensor and tacho interface
  - DC-Brake
  - Isolated JTAG (in Rev 2)

- **Rev.1** – prototypes - Available per specific business opportunities
- **Rev.2** – productization – in progress, to be available in Q1 2014
as a Real-time Monitor
PC Master functionality categories:

- **Monitor functions:**
  watching on-board memory locations (board application variables) in various formats:
  - textual in the tabular form
  - real-time charts of the values (oscilloscope via RS232)
  - graphs of high-speed recorded data (on board memory oscilloscope)

- **Control functions:**
  - setting the variable values asynchronously to the on-board application
  - stimulating the variable values according to specific time-table
  - sending “user commands” as an official message to the board application
Freemaster as a Real-time Monitor

- **Connects to an embedded application**
  - SCI, UART
  - JTAG/EOnCE (DSC, Kinetis)
  - BDM (HCS08, HCS12)
  - CAN Calibration Protocol
  - Ethernet, TCP/IP
  - Any of the above remotely over the network

- **Enables access to application memory**
  - Parses ELF application executable file
  - Parses DWARF debugging information in the ELF file
  - Knows addresses of global and static C-variables
  - Knows variable sizes, structure types, array dimensions etc.
Control Page Example

3-Phase ACIM V/Hz Constant Slip Control

Application Status
Fault
Manual Control

PWM ON/OFF

Designed by Roznov CSC
Transportation and Standard Products Group
Roznov pod Radhostem, Czech Republic
Scope Example

- similar to the classical hardware oscilloscope
- variables read in real-time
- sampling time limited by communication data link
Recorder Example

- variables recorded by the embedded-side timer periodic ISR
- after requested number of samples data stored in Recorder buffer
- sample very fast actions
- buffer download can be defined
Stimulator Example
What is **FreeMaster**?

**Application control and monitor**
- Live graphs, variable watches, and graphical control page

**Real-time operation monitor**

FOR YOUR EMBEDDED APPLICATION

![Images of FreeMaster software interfaces](image-url)
What is QuickStart?

Quick Start = Easy-to-use SW Development Environment for DSC

- **QuickStart includes**
  - Set of Low-level Drivers for all Peripheral Modules
  - Ready-to-use Project Templates (“Project Stationery”)
  - Graphical Configuration Tool
  - Sample Applications
  - User Manual

- **QuickStart**
  - Designed according to customer needs
  - Supports all DSC’s including latest 56F802xxx/4xxx
  - Mandatory development tool for key appliance customers (Electrolux, Indesit, Miele, DiehlAKO, Emerson, PowerOne, etc)
Low-level Drivers

- **Quick Start Low-level Drivers**
  - Full control over and full access to all processor resources
  - Unifies access to peripheral memory space (**ioctl** call)
  - Registers are not accessed directly, although this is still possible
  - **ioctl** calls are optimally compiled macros or functions

```c
ioctl(SCI_0, SCI_SET_BAUDRATE, SCI_BAUD_9600)
```

### Module identifier

### Command to perform

### Command Parameter
ioctl (Input Output Control) Commands

• general syntax :

```
ioctl( module_ID, cmd_name, cmd_spec_param );
```

• module_ID – module identifier
  
  - Predefined symbolic constant corresponding to names of peripheral modules
    
    ▪ Example: GPIO_A, GPIO_B, ADC, ADC_A, ADC_B, PWM, PWM_A, PWM_B, COP, etc.

• cmd_name – specifies action performed on a peripheral module
  
  - Command is depended to performed operation
  
  - Example for pwm.h: PWM_SET_PRESCALER, PWM_SET_RELOAD_FREQUENCY,
    PWM_FAULT_INT_ENABLE

• cmd_spec_param – command specific parameter
  
  - Specifies other data required to execute the command
  
  - Example for pwm.h:
    
    ▪ #define PWM_PRESCALER_DIV_1             0
    ▪ #define PWM_PRESCALER_DIV_2             1
    ▪ #define PWM_PRESCALER_DIV_4             2
    ▪ #define PWM_PRESCALER_DIV_8             3
    ▪ Etc.
Graphical Configuration Tool

• **Features:**
  - Edits post-reset processor configuration graphically
  - Configuration saved/ **read** from a single ANSI C header file
  - GUI to configuration bits of all peripheral module registers
  - Possible conflict warnings
  - Pin-out view of processor I/O pins
Graphical Configuration Tool

- Used to edit the ANSI C-compatible application configuration header file (appconfig.h)
- appconfig.h contains a single macro constant per peripheral register

Ctrl+F10 invoked GCT opens the appconfig.h for a current project

#include "appconfig.h"
#define used to initialize peripherals

Read & Write access to appconfig.h
Graphical Configuration Tool

Different Control Page for each Peripheral Module

Module Configuration Page

Clocks Summary

Registers Summary

Peripheral Modules Tree

Warnings Summary
Graphical Configuration Tool

Direct Register Value View
Graphical Configuration Tool

- Conflict Warnings

Warning detail
GPIO A6 mode bad

More detailed warning description
Timer Pin #0 is not set to Timer mode in GPIO_A6

More detailed warning description
Module QT_A0 is configured for use but its peripheral clock is disabled
Embedded Software Libraries
S/W Algorithms for Sensorless Vector Control

- FW Error Calculator
- Field Control
- d-current Control
- Inverse Park Transformation
- SVM
- d,q
- u_d
- α,β
- u_α
- u_β
- Clarke Transformation
- Park Transformation
- Fast Loop (faster) ~50-100μs

- Ramp
- Speed Control
- q-current Control
- Σ
- u_q
- Σ
- u_d
- Fast Loop (faster) ~50-100μs

- Slow Loop (slower) ~ 1-5ms
- Tracking Observer
- BEMF Observer
- θ
- ω

- Inverter
- Load

- Inverter
- Load

- Inverter
- Load
Embedded Software Libraries

- **Set of basic trigonometric, general math, filter & motor control algorithms** as the building blocks for the motor control applications

- Provided in highly optimized layered architecture, support of **16/32-bit fixed-point** and **single precision floating point** arithmetic

- Matlab/Simulink models included in the package

- Delivered as object file for the **evaluation purposes for free**, **production ready** version by June ‘13
Math and Motor Control Library Set

Note:
- MC Lib for 56800E – Math functions included into the individual algorithms
- MC Lib for 56800EX - Math functions separated into MLIB
# Math and Motor Control Library Set – Contents

## MLIB
- Absolute Value, Negative Value
  - MLIB_Abs, MLIB_AbsSat
  - MLIB_Neg, MLIB_NegSat
- Add/Subtract Functions
  - MLIB_Add, MLIB_AddSat
  - MLIB_Sub, MLIB_SubSat
- Multiply/Divide/Add-multiply Functions
  - MLIB_Mul, MLIB_MulSat
  - MLIB_Div, MLIB_DivSat
  - MLIB_Mac, MLIB_MacSat
  - MLIB_VMac
- Shifting
  - MLIB_ShL, MLIB_ShLSat
  - MLIB_ShR
  - MLIB_ShBl, MLIB_ShBSat
- Normalisation, Round Functions
  - MLIB_Norm, MLIB_Round
- Conversion Functions
  - MLIB_ConvertPU, MLIB_Convert

## GFLIB
- Trigonometric Functions
  - GFLIB_Sin, GFLIB_Cos, GFLIB_Tan
  - GFLIB_Asin, GFLIB_Acos, GFLIB_Atan, GFLIB_AtanYX
  - GFLIB_AtanYXShifted
- Limitation Functions
  - GFLIB_Limit, GFLIB_VectorLimit
  - GFLIB_LowerLimit, GFLIB_UpperLimit
- PI Controller Functions
  - GFLIB_ControllerPIr, GFLIB_ControllerPIrAW
  - GFLIB_ControllerPIp, GFLIB_ControllerPIpAW
- Interpolation
  - GFLIB_Lut1D, GFLIB_Lut2D
- Hysteresis Function
  - GFLIB_Hyst
- Signal Integration Function
  - GFLIB_IntegratorTR
- Sign Function
  - GFLIB_Sign
- Signal Ramp Function
  - GFLIB_Ramp
- Square Root Function
  - GFLIB_Sqrt

## GDFLIB
- Finite Impulse Filter
  - GDFLIB_FilterFIR
- Moving Average Filter
  - GDFLIB_FilterMA
- 1st Order Infinite Impulse Filter
  - GDFLIB_FiltterIR1Init
  - GDFLIB_FiltterIR1
- 2nd Order Infinite Impulse Filter
  - GDFLIB_FiltterIR2Init
  - GDFLIB_FiltterIR2

## GMCLIB
- Clark Transformation
  - GMCLIB_Clark
  - GMCLIB_ClarkInv
- Park Transformation
  - GMCLIB_Park
  - GMCLIB_ParkInv
- Duty Cycle Calculation
  - GMCLIB_SvmStd
- Elimination of DC Ripples
  - GMCLIB_ElimDCBusRip
- Decoupling of PMSM Motors
  - GMCLIB_DecouplingPMSM

## ACLIB/AMCLIB
- Angle Tracking Observer
- Tracking Observer
- PMSM BEMF Observer in Alpha/Beta
- PMSM BEMF Observer in D/Q

## Delivery Content
- User Manuals
- Header files
- Compiled Library File
- License File (to be accepted at install time)
## MCU Math and Motor Control Library

<table>
<thead>
<tr>
<th>Target Platform</th>
<th>CodeWarrior</th>
<th>Keil</th>
<th>IAR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CW8.3</td>
<td>CW10.5</td>
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<td>56800E</td>
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<td>56800E/EX</td>
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<td>ColdFireV1</td>
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<td>CortexM4 FixPoint (K, KV)</td>
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<tr>
<td>CortexM4 Float (K, KV)</td>
<td>N/A</td>
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</tbody>
</table>

Product related web pages:

[www.freescale.com/FSLESIL](http://www.freescale.com/FSLESIL)
Digital Power Control Library for DSC

- **Library Provides:**
  - Power Factor Correction
  - AC-DC converter
  - DC-DC Converter
  - DC-AC Inverter
  - Solar Inverter

- **Algorithms:**
  - ASM coded & optimized
  - fully tested using Matlab

- **Compensation block :**
  - PI compensation Kp+Ki/s
  - PID Compensation Kp+Ki/s+s*Kd
  - PI+Lowpassfilter (Kp+Ki/s)*((s+a)/((s+b))
  - 2P 2Z Compensation (s+a)*(s+b)/((s+c)*(s+d))
  - 3P 3Z Compensation (s+a)*(s+b)*(s+x)/((s+c)*(s+d)*(s+y))
Digital Control library  Future ....

- Same compensation block library will be develop for Kinetis

- MPPT algorithm library for solar application
  - Modified P&O method
  - PI based control loop
  - Input variable and drive output is in fraction to optimize number resolution

- PFC control loop library
  - Control loop co-efficient is calculated in library
  - User need to provide passive component value and switching and sampling frequency
  - Average current mode control is implemented
  - Drive output is in fraction format
IEC60730 Safety Libraries
Application Safety – Home Appliance

- From Oct 2007, home appliances to be sold in Europe have to comply with IEC60730 standard
- The IEC60730 standard defines the test and diagnostic methods that ensure the safe operation of embedded control hardware and software for household appliances
- Intention of the regulation is to implement features that will avoid failure or at least ensure that any failure in the appliance does not present a safety hazard to the user.
- **Semiconductor suppliers must consider the impact of these standards on home appliance manufacturers when developing microelectronics for these devices**
- The standard is applied to overall solution
  - Hardware
  - Software
- The standard classifies applicable equipment into three categories:
  - Class A
  - Class B
  - Class C
- Implemented safety features (software and hardware features) have to pass the certification process at the certification authority
IEC 60730 Classification of Appliances

- **Class A** are products with no feature/function that can harm a human being.
  - room thermostats, humidity controls, lighting controls, timers and switches.

- **Class B**
  - IEC 60730-1: Control functions intended to prevent unsafe operation of the controlled equipment.
    - washing machines, dishwashers, dryers, refrigerators, freezers and cookers/stoves
  - **IEC 60335-1:** Software that includes code intended to prevent hazards if a fault, other than a software fault occurs in the appliance

- **Class C**
  - IEC 60730-1: Control functions which are intended to prevent special hazards (e.g. Explosion of the controlled equipment).
    - automatic burner controls and thermal cut-outs for closed water heater systems (unvented).
  - **IEC 60335-1:** Software that includes code intended to prevent hazards without the use of other protective devices.
IEC 60730 – Class B

• Recommended self-diagnostic tests for microcontrollers in Class B

- Diagnostic of CPU registers
- Diagnostic of PC (program counter)
- Diagnostic of watchdog
- Memory testing – Flash
- Memory testing – RAM

- Runtime diagnostic of stack failure
- Diagnostic of interrupt handling and execution
- Diagnostic of clock frequency (accuracy)
- Diagnosis of abnormalities in external interface (communications)
- Runtime diagnostic of critical variables of control algorithm
- Etc. (depends on the application)

Provided by Freescale as a certified library
Test Routines Timing 56F8037

2.5μs

| 29ms | 50ms | 40μs | 84.4ms | 1.9ms |

COP

Reset & PLL lock

Registers

Flash 32kW

RAM 4kW

Standard clock source 32MHz
Approved IEC60730 safety s/w routines from Freescale

<table>
<thead>
<tr>
<th>Microcontroller</th>
<th>IEC60730 Class B</th>
<th>IEC60730 Class C</th>
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<tbody>
<tr>
<td>MC9S08ACxx</td>
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<td>Available</td>
</tr>
<tr>
<td>MCF51xx</td>
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<td>not planned</td>
</tr>
<tr>
<td>MC56F8xx/80xx</td>
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</tr>
<tr>
<td>MC56F82xx/84xx</td>
<td>Certified in June 2013</td>
<td>not planned</td>
</tr>
<tr>
<td>Kinetis K, KE, KL, KV, KM (CM0, CM4, CM4 Float)</td>
<td>Certified in June 2013</td>
<td>not planned</td>
</tr>
</tbody>
</table>

“All pieces have been certified by VDE to help accelerate manufacturer development”

FSL Web page: [IEC 60730 Safety Standard for Household Appliances](#)
Typical use cases
Sensorless Control of 3-ph PMSM Motor

- Typical configuration:
  - 6 PWM outputs
  - Min. 5 ADC channels
  - Analog measurements in one PWM cycle
    - 2 x 2 currents simultaneously
      - 2 currents at the same instant for calibration
      - 2 currents at the same instant for FOC algorithm
    - Vdc bus (DC-bus voltage)
    - 2 ADCs run simultaneously
    - PWM to ADC synchronization – 3 events in one PWM cycle for FOC

**Typical Use**
Appliance Drives (washer, dishwasher, dryer, compressor, pump)

**Recommended Devices**
MC56F82xxx
Sensorless Control of 3-ph PMSM Motor + PFC

- **Typical configuration:**
  - 6 PWM outputs
  - One ADC module - Min 4 ADC channels
  - Analog measurement in one PWM cycle
    - 1 current for calibration
    - 2 currents for FOC algorithm
    - V dc bus
  - PWM to ADC synchronization – 4 events in one PWM cycle for FOC

- **PFC support**
  - 1 or 2 PWM outputs – PWM freq. about 100kHz
  - One ADC module - 2 ADC channels
  - Analog measurement in one PWM cycle for PFC
    - PFC current – input current
    - Voltage – V input

**Recommended Devices**

- MC56F82xxx

**Typical Use**

- High power drives
3-in-1 (2x PMSM + PFC)

Touch Graphic LCD

UART DRIVER
Communication State Machine

16-bit ADC DRIVER
Input voltage

PWM A SM 3 DRIVER
PFC current

PWM A SM 0, 1, 2 DRIVER
PWM

PWM B SM 0, 1, 2 DRIVER
PWM

12-bit ADC DRIVER

Motor 1 State Machine
PFC switch, voltage command
PFC status
M1 switch, speed command
M1 status

Motor 2 State Machine
PFC status
M2 switch, speed command
M2 status

Application State Machine
Switch
Compressor speed
Status, recorder

Recommended Devices
MC56F84xxx

Typical Use
AirCon, Washers
Multi-phase DC/DC Buck Converter

- Concentrated control multiple converters, reduce IC counts
- Simplify system power management by one-chip architecture
- Reduces the ripple current in the input bus capacitor, alleviating electrical overstress on capacitor
- High-resolution and flexible PWM supports high switching frequency and interleaved parallel, suitable small volume applications
- High-speed ADC and high-performance core support real-time control multiple converters in one chip

Recommended Devices

MC56F82xxx, MC56F84xxx
Q & A
Designing with Freescale

Tailored live, hands-on training in a city near you

2014 seminar topics include

• QorIQ product family update
• Kinetis K, L, E, V series MCU product training

freescale.com/DwF