High Speed I/O Interfaces:

**USB 3.0**

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Session Introduction

• Introduction of USB 3.0
  – Understand USB 3.0 architecture
  – The differences between USB 3.0 and USB 2.0

• USB 3.0 on LS1

• Time allocation
  – 45 min presentation
  – 5 min Q&A

• Author
  – Jimmy Zhao, PE, System and Application Engineer, Digital Networking
  – SME for USB, SPI, SDHC
Session Objectives

• After completing this session you will be able to:
  – Know the differences between USB 3.0 and USB 2.0
  – Understand USB 3.0
    ▪ USB 3.0 Feature
    ▪ Layered Protocol Architecture
      • Details on Protocol layer
      • Details on Link layer
      • Details on Physical layer
  – USB 3.0 on LS1
    ▪ Data structure and Memory map
Agenda

• USB 3.0 Introduction
  − Features
  − Architecture
  − Cable/Connectors
  − Layered Protocol Architecture
    ▪ Protocol Layer
    ▪ Link Layer
    ▪ Physical Layer

• LS1 USB Information
  − Introduction
  − Data structure and Register memory map
USB 3.0 Introduction / Features

- 10x performance increase over USB 2.0
  - 5 Gbps vs. 480 Mbps

- Backward compatible
  - Legacy devices continue to work when plugged into new host connector
  - New devices work when plugged into legacy systems albeit at USB 2.0 speeds
  - Existing class drivers continue to work

- Same USB Device Modes
  - Pipe Model
  - USB Framework
  - Transfer Types

- Power Efficient
  - Provides excellent power characteristics (especially for idle links)
    - Both on the device and platform
  - Eliminate need for polling

- Extensible
  - Protocol designed to efficiently scale up
Agenda

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  - Features
  - Architecture
  - Cable/Connectors
  - Layered Protocol Architecture
    - Protocol Layer
    - Link Layer
    - Physical Layer

- LS1 USB Information
  - Introduction
  - Data structure and Register memory map
USB 3.0 Architecture

- Dual-bus Architecture SuperSpeed bus operates concurrently with USB2.0
  - Electrically/mechanically backward and forward compatible
  - Devices discovered / configured at fastest signaling rate
  - Hubs provide additional connection points

- SuperSpeed USB
  - Dual simplex signaling
  - Packets routed to device
  - Hubs store and forward
  - Asynchronous notifications
USB 3.0 Architecture (continued)

- Dual-bus architecture for backward compatibility
- USB 3.0 Host
  - Supports SS and USB 2.0
- USB 3.0 Hub
  - Supports SS and USB 2.0
- USB 3.0 Device
  - Supports SS and HS (FS/LS optional)
  - Concurrent SS and USB 2.0 traffic is not allowed
- FSL USB 2.0 Host: works for couple USB 3.0 HDDs
Agenda

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  - Features
  - Architecture
  - Cable/Connectors
  - Layered Protocol Architecture
    ▪ Protocol Layer
    ▪ Link Layer
    ▪ Physical Layer

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  - Data structure and Register memory map
USB 3.0 Connectors

- Standard-A Connector
- Standard-B Connector
- Micro-AB/A
USB 3.0 Cable

- Embeds physical USB2 bus in parallel with the USB3 SuperSpeed bus
- USB 2.0 and 3.0 packets operate independently

Note:
- STP: Shield Twisted Pair
- UTP: Unshield Twisted Pair
Agenda

• USB 3.0 Introduction
  - Features
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  - Layered Protocol Architecture
    ▪ Protocol Layer
    ▪ Link Layer
    ▪ Physical Layer
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USB 3.0 Layered Protocol Architecture
USB 3.0 Protocol Layer

• Convert the requests from the functional layer into transactions consisting of packets
• Manage the end-to-end data flow between the host and the device
• Reliability for packets
  – Sending Acknowledgement packets
  – Request/retransmit lost/corrupted data
  – Packet payload (not in Link)
• Power management
  – Enter reduced power states after a NRDY response
  – Unicast vs. broadcast packets
• Bandwidth management
  – Stream support for performance
  – Asynchronous notification ERDY be device vs. host polling
USB 3.0 Protocol Layer – Packets

• Start from transmitter protocol layer terminated at the receiver protocol layer
• Application data embedded in the data packet Payload
• Host initiates all data transfers.
• Header and Data packet Payload
  – Address triple: device address, endpoint number, direction
  – Route string: the path between the host and the device
• Device response
  – Response immediately: device => host
  – Deferred response: restarted synchronously by the device
USB 3.0 Protocol Layer – Packets Format

- 16-byte Header
  - 12 bytes header information

- Four packet types:
  - Link Management Packet (LMP)
  - Transaction Packet (TP)
  - Data Packet (DP)
  - Isochronous Timestamp Packet (ITP)

- Only DP has a Data Packet Payload (DPP) besides Packet Header

- LMP and ITP not routable
USB 3.0 Protocol Layer – Packet Types

• Link Management Packet (LMP)
  – Sent directly to connected ports between link partners
  – No addressing information
    ▪ Not routable
  – Used to manage the link
  – Subtypes
    ▪ Set Link Function
    ▪ U2 Inactive Timeout
    ▪ Vendor Device Test
    ▪ Port Capability
    ▪ Port Configuration
    ▪ Port Configuration Response
USB 3.0 Protocol Layer – Packet Types

• Isochronous Timestamp Packet (ITP)
  - Only sent out when root port link is in U0 around bus interval boundary
  - Replace SOF/uSOF in USB 2.0
  - Multicast to all active links, no routing information
  - Delayed bit is set when ITP is delayed by Hub
  - Send host SS 125 uSec bus interval/service interval timing to any device
  - Devices:
    ▪ Not respond
    ▪ Lock an internal time base to the host timing
    ▪ Ignore it if delayed flag set
    ▪ Needs to be in U0 if expecting ITP
USB 3.0 Protocol Layer – Packet Types

• Transaction Packet (TP)
  – Control the data flow, configure devices and hubs
  – Subtypes
    ▪ ACK
    ▪ NRDY
    ▪ ERDY
    ▪ STATUS
    ▪ STALL
    ▪ DEV_NOTIFICATION
    ▪ PING
    ▪ PING_RESPONSE
USB 3.0 Protocol Layer – Types of Transaction Packets

- **ACK(0001b)**
  - IN: Received without error
  - OUT: Rx buffers available

- **NRDY(0010b)**
  - IN: No data packets available
  - OUT: Rx buffers unavailable
  - Non-ISO device EP

- **ERDY(0011b)**
  - IN: Data packets available now
  - OUT: Rx buffers available now
  - Non-ISO device EP
USB 3.0 Protocol Layer – Types of Transaction Packets (continued)

- **STALL (0101b)**
  - EP halted / Control transfer invalid
- **DEV_NOTIFICATION (0110b)**
  - Asynchronous change in a device / interface state
    - Function Wake
    - Latency Tolerance
    - Bus Interval Adjustment
- **STATUS (0100b)**
  - Status change of a control transfer
- **PING (0111b)**
  - Ensure device is in U0 before sending the ISO packets
- **PING RESPONSE (1000b)**
  - Confirm device still reminds in U0 until the ISO packets are received
  - Send for every PING
USB 3.0 Protocol Layer – Flow Control

• It is in flow control when a device EP is not ready to send/receive data
• Not apply to Isochronous Eps
• Flow control mechanisms:
  – Sends NRDY/ERDY
  – IN
    • Sends a DP with the EOB = 1
  – OUT
    • Sends an ACK with NumP = 0
• Terminating flow control
  – Device sends an ERDY

NumP:
IN: number of packets requested
OUT: Buffer space availability
USB 3.0 Protocol Layer – Transactions

• Bulk Transactions
• Control Transactions
  – Same as USB 2.0
    ▪ 3 or 2 stages: Setup, Data (optional), Status
  – Max packet size: 512 bytes
• Interrupt Transactions
  – Max packet size: 1024 bytes
  – For infrequent data transfer with guaranteed bounded latency
  – Up to burst of 3 packets / interval
• Isochronous Transactions (No Retry)
  – Max packet size: 1024 bytes
  – Up to 48 packets / interval (375 MB/s)
  – Interval: $125 \mu s \times 2^{(B\text{interval}-1)} \Rightarrow (125 \mu s, \ldots, 4 s)$
USB 3.0 Protocol Layer – Bulk Transaction

• Up to 16 bursts
• Support streams
• Max packet size: 1024 bytes
• Guarantee error-free delivery of data
  – Error detection
  – Retry
• Flow control
• Basic Retry
  – Set Seq# = Seq# of the bad/missing data packet
## USB 3.0 Protocol Layer – Bulk Transaction (Burst)

- Host knows max. burst size for EP during enumeration
- Max. number of packets sent without getting an ACK is limited:
  - Min of \(\{(\text{Max. burst size}), \text{NumP}\}\)
- NumP can be incremented anytime by the host or a device
- Burst terminate
  - NumP = 0
  - A short packet

### Burst Retry Sequence

**IN Burst Retry Sequence**

<table>
<thead>
<tr>
<th>Host Tx</th>
<th>Host Rx</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACK(0,4)</td>
<td>DATA(0, -)</td>
</tr>
<tr>
<td>ACK(1,4)</td>
<td>DATA(1, -)</td>
</tr>
<tr>
<td>ACK(2,4)</td>
<td>DATA(2, -)</td>
</tr>
<tr>
<td>ACK(2,4)</td>
<td>DATA(3, -)</td>
</tr>
<tr>
<td>ACK(2,4)</td>
<td>Discard</td>
</tr>
<tr>
<td>ACK(3,4)</td>
<td>DATA(4, -)</td>
</tr>
<tr>
<td>ACK(4,4)</td>
<td></td>
</tr>
<tr>
<td>ACK(5,4)</td>
<td></td>
</tr>
</tbody>
</table>

**OUT Burst Retry Sequence**

<table>
<thead>
<tr>
<th>Host Tx</th>
<th>Host Rx</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATA(0, -)</td>
<td>ACK(1,4)</td>
</tr>
<tr>
<td>DATA(1, -)</td>
<td>ACK(2,4)</td>
</tr>
<tr>
<td>DATA(2, -)</td>
<td>ACK(3,4)</td>
</tr>
<tr>
<td>DATA(3, -)</td>
<td>ACK(4,4)</td>
</tr>
<tr>
<td>DATA(4, -)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Data**
  - \(\text{DATA}(n, -)\)
- **ACK**
  - \(\text{ACK}(n, m)\)
- **Error**
  - Discard
- **Retry Set**
USB 3.0 Protocol Layer – Bulk Transaction (SS Streaming)

- Multiplexing multiple independent logic data streams
- Up to 65533 streams
- Managed by the Stream Protocol
  - Host or a device setup CStream ID (Current Stream) associated with an EP
  - CStream ID
    - Host: To select the command/operation specific EP buffers for data transfer
    - Device: To select the Function Data buffers
USB 3.0 Link Layer

- Manage the port-port flow of data between the host and the device
- Manage/control the logic portion of the link: reliability, flow control, data integrity, link power management

- Link Training
  - Link Training and Status State Machine (LTSSM)
  - Bit-Lock, Symbol-Lock, and Rx Equalization

- Power Management
  - 4 Link Power States: U0, U1, U2, U3
  - Low Frequency Periodic Signaling (LFPS)

- Error Handling
  - Bit, Link, Packet errors
USB 3.0 Link Layer – Power Management

<table>
<thead>
<tr>
<th>Link State</th>
<th>Description</th>
<th>Key Characteristics</th>
<th>State Transition Initiator</th>
<th>Exit Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td>U0</td>
<td>Link Active</td>
<td>Operational State</td>
<td>N/A</td>
<td>NA</td>
</tr>
<tr>
<td>U1</td>
<td>Link Idle - Fast Exit</td>
<td>RX &amp; TX Circuit Quiesced</td>
<td>Hardware</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- PLL remains on / Clock gating / P1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U2</td>
<td>Link Idle - Slow Exit</td>
<td>Clock Generation Circuit Quiesced</td>
<td>Hardware</td>
<td>μs to ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- PLL can be turned off / Clock gating / P2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U3</td>
<td>Link Suspend</td>
<td>Portions of device power removed</td>
<td>Entry: Software</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Clock generation circuit can be turned off</td>
<td>Exit: Hardware or Software</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>/ Clock gating / P3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- U0 to U1 entry based on
  - Downstream port inactivity time
    - Port_U1_TimeOut (Can be as low as 10us)
  - Device hardware initiated
    - Based on implementation specific knowledge

- In both cases - Always initiated with Link command
  \texttt{LGO\_U1 -> LAU}
USB 3.0 Link Layer – Link States

- **Connection**
  - Idle: Rx.Detect

- **Link Training**
  - Polling states

- **Normal State**: U0
  - Descriptors

- **Low Power States**
  - U1
  - U2
  - U3
## USB 3.0 Link Layer – Link Training

<table>
<thead>
<tr>
<th>Packet</th>
<th>TERM State</th>
<th>Time Stamp</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>ON</td>
<td>7.235.026.592</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Packets</th>
<th>Type</th>
<th>Duration</th>
<th>ELdts</th>
</tr>
</thead>
<tbody>
<tr>
<td>972</td>
<td>LFPS</td>
<td>1.016 us</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Packets</th>
<th>Type</th>
<th>Duration</th>
<th>ELdts</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>LFPS</td>
<td>1.064 us</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Packet</th>
<th>IPS</th>
<th>Count</th>
<th>Time</th>
<th>Time Stamp</th>
</tr>
</thead>
<tbody>
<tr>
<td>1001-2654</td>
<td></td>
<td>D21</td>
<td>7.240.586.928</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Packets</th>
<th>Type</th>
<th>Duration</th>
<th>ELdts</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>TS1 Data</td>
<td>1.128 us</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Packet</th>
<th>Link Config</th>
<th>Loopback</th>
<th>Scrambling</th>
</tr>
</thead>
<tbody>
<tr>
<td>135627-135657</td>
<td>Normal</td>
<td>Off</td>
<td>On</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Packet</th>
<th>Link Config</th>
<th>Loopback</th>
<th>Scrambling</th>
</tr>
</thead>
<tbody>
<tr>
<td>135528-135565</td>
<td>Normal</td>
<td>Off</td>
<td>On</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Packet</th>
<th>TS1 Data</th>
<th>Time</th>
<th>Time Stamp</th>
</tr>
</thead>
<tbody>
<tr>
<td>135559-183082</td>
<td></td>
<td>14.000 ns</td>
<td>7.244.957.816</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Packet</th>
<th>TS2 Data</th>
<th>Time</th>
<th>Time Stamp</th>
</tr>
</thead>
<tbody>
<tr>
<td>135669-183081</td>
<td></td>
<td>18.000 ns</td>
<td>7.245.958.310</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Packet</th>
<th>TS2 Data</th>
<th>Time</th>
<th>Time Stamp</th>
</tr>
</thead>
<tbody>
<tr>
<td>183003-183113</td>
<td></td>
<td>18.000 ns</td>
<td>7.245.722.284</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Packet</th>
<th>TS2 Data</th>
<th>Time</th>
<th>Time Stamp</th>
</tr>
</thead>
<tbody>
<tr>
<td>183084-183126</td>
<td></td>
<td>956.000 ns</td>
<td>7.245.722.302</td>
</tr>
</tbody>
</table>
USB 3.0 Link Layer – Header Packet Framing

- Header Packet Framing (20 Bytes)
  - 4 bytes of Packet start framing
    - SHP, SHP, SHP, EPF
  - 12 bytes Packet Header
    - LMPs, TPs, ITPs, DPHs
  - 2 byte CRC
  - 2 bytes Link Control Word
USB 3.0 Link Layer – Link Command

- For data integrity, flow control, link power management
- Only from Transmitter link layer to Receiver link layer

<table>
<thead>
<tr>
<th>Link Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LGOOD_n</td>
<td>Good header packet</td>
</tr>
<tr>
<td>LRTY</td>
<td>Retry header packet</td>
</tr>
<tr>
<td>LBAD</td>
<td>Bad header packet</td>
</tr>
<tr>
<td>LCRD_x</td>
<td>Rx header buffer credit index</td>
</tr>
<tr>
<td>LGO_U1/2/3</td>
<td>Request entry to U1/2/3</td>
</tr>
<tr>
<td>LAU</td>
<td>Accept PM request</td>
</tr>
<tr>
<td>LXU</td>
<td>Reject PM request</td>
</tr>
<tr>
<td>LPMA</td>
<td>LAU handshake</td>
</tr>
<tr>
<td>LUP/LDN U0</td>
<td>Link Up/Down</td>
</tr>
</tbody>
</table>

Packet Acknowledgement and Error Recovery
Packet Flow Control
Link Power Management

8-Symbol Link Command
MSB
LSB (transmitted first)
Start Link Command
SLC
SLC
SLC
EPF
End Packet Framing
Link Command Word
Link Command Information

byte 1 byte 0
CRC-5 Link Command Information
USB 3.0 Link Layer – Link Command

• LGOOD_n
  - Everything Good

• LBAD
  - Invalid header packet
  - Bad/corrupted CRC
  - Resend all header packets after the last one with LGOOD_n

• LRTY
  - Send before resending the 1st header packet after LBAD

• LCRD_x (x: A, B, C, D) Header Buffer Credit index
  - Indicate a single Rx Header Buffer Credit is available
  - Sent after received packet meet:
    ▪ LGOOD_n is sent
    ▪ Header packet has been processed, a Rx Header Buffer Credit is available
USB 3.0 Link Layer – Link Command

- **LGO_U1/U2/U3**
  - Requesting enter to U1/U2/U3
  - Upstream port must accept U3
- **LAU**
  - A port accepting the request to enter U1/U2
- **LXU**
  - A port rejecting the request to enter U1/U2
- **LPMA**
  - A port receiving LAU
- **LUP**
  - Device is in U0
  - Sent by an upstream port every 10 uS when there is no packets or other link commands to be sent
USB 3.0 Link Layer – Link Command, Retry

**Tx Link Partner**
- **Tx Header Buffer**
- **Tx Header Sequence Number:** 1
- **Ack’ed Tx Header Sequence Number:** 1
- **Remote Rx Header Buffer Credit:** 4
- **Rx LCRD_x Index:** B

**Rx Link Partner**
- **Rx Header Buffer**
- **Rx Header Sequence Number:** 1
- **Local Rx Header Buffer Credit:** 4
- **Remote Rx LCRD_x Index:** B

**Annotations:**
- HP, HSEQ#=0
- LBAD
- LRTY
- HP, HSEQ#=0
- LCRD_A
USB 3.0 Physical Layer

- Actual physical connection between 2 ports
  - Two differential data pairs
    - One Transmit
    - One Receive
- 8b/10b encode/decode
  - ANSI X3.230-1994
- Scramble/descramble
- Spread Clock CDR (Clock Data Recovery)
- Elasticity Buffer/Skips
- Low Frequency Period Signaling (LFPS)
USB 3.0 Physical Layer (continued)

Transmitter Functions

D-Code/K-Code

x 8

D/K

Scrambler (D only)

x 8

Core Clock

8b/10b Encoding

x 10

Parallel to Serial

Bit Clock

x 1

Transmitter Differential Driver

D+ D-

Receiver Functions

In

D+ D-

Differential Receiver and Equalization

Bit Rate

Clock Recovery Circuit

Recovered Bit Clock

Data Recovery Circuit (DRC)

x 1

RxPolarity

Serial to Parallel

K28.5 Detection

RxValid

x 10

Recovered Symbol Clock

Elastic Buffer

RxDataK

RxCodeErr

RxDispErr

x 10

Core Clock

Desynchronizing (D only)

x 8
USB 3.0 Physical Layer - PIPE

- PCLK from PHY to MAC: 500/250/125 MHz
- Rx and Tx Data: 8-, 16-, or 32-bits
- Rx and Tx DataK: 1-, 2- or 4-bits
- Command Signals: 12- or 16-bits
  - PHYMode, Rxdetect/loopback, TxElecIdle, RxPolority, TxEqua, TxComplicance, Rate, TxMargin, TxDeep, RxTerm, TxSwing, etc.
- Status Signals: 6- or 7-bits
  - PHYStatus, RxValid, RxStatus, RxElecIdle, PowerPresent
Agenda

- **USB 3.0 Introduction**
  - Features
  - Architecture
  - Cable/Connectors
  - Layered Protocol Architecture
    - Protocol Layer
    - Link Layer
    - Physical Layer

- **LS1 USB Information**
  - Introduction
  - Data structure and Register memory map
LS1 Architecture

• One USB 2.0 with ULPI (UTMI+Low Pin Interface)
• OTG (On The Go) 2.0
• USB Dual-Role Controller
• One USB 3.0 with internal PHY
  - Super-speed (SS) – 5 Gbps
  - High-Speed (HS) – 480 Mbps
  - Full-Speed (FS) – 12 Mbps
  - Low-Speed (LS) – 2 Mbps (only for USB 2.0 host mode)
  - Support 8 programmable, bidirectional endpoints
• Compatible with xHCI spec
USB 3.0 Controller and PHY

SoC Bus

- System CPU
- System Memory
- Application

USB Controller
- Bus Interface, Registers, List Processor
- USB 3.0 MAC & LINK
- Buffer Management
- USB 2.0 MAC

USB PHY
- SuperSpeed Function (PIPE 3)
- High-Speed Function (UTMI)

Tx Data FIFO RAM
Rx Data FIFO RAM
Descriptor Register Cache RAM

Power supplies, Clocks, …

tx <#> _p
tx <#> _m
rx <#> _p
rx <#> _m

DP <#>, DM <#>
USB 3.0 eXtensible Host Controller Interface (xHCl)

CCSR
(Configuration, Control, and Status Register)
USB Base Address (310_0000H)
USB 3.0 Controller Memory Map/Registers

- USB 3.0 Registers
  - 32-bits wide
  - Address: 32-bit block aligned
  - Access the register
    - Only 32-bit units
    - 8-bit or 16-bit illegal

- Global Registers
- Device Registers
- OTG Registers
- xHCI Host Registers
USB 3.0 Host Memory Map/Registers

<table>
<thead>
<tr>
<th>OFFSET</th>
<th>ACRONYM</th>
<th>External Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0000</td>
<td>CAPLENGTH</td>
<td></td>
</tr>
<tr>
<td>0x0004</td>
<td>HCSPARAMS1</td>
<td></td>
</tr>
<tr>
<td>0x0008</td>
<td>HCSPARAMS2</td>
<td></td>
</tr>
<tr>
<td>0x000C</td>
<td>HCSPARAMS3</td>
<td></td>
</tr>
<tr>
<td>0x0010</td>
<td>HCCPARAMS</td>
<td></td>
</tr>
<tr>
<td>0x0014</td>
<td>DBOFF</td>
<td></td>
</tr>
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<td>Rsvd</td>
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**HOST REGISTERS**

**eXtensible Host Controller Capability Registers**

**HOST CONTROLLER OPERATIONAL REGISTERS**

- Rsvd:20'hx
- Rsvd:16'hx
- Rsvd:32'hx
- Rsvd:13'hx
- Rsvd:32'h0
- Rsvd:6'hx
- MaxSlotsEn:8'b0

**ACCESS TYPES**

- R_W
- RO
- RU
- WO
- R_WS_SC
- R_SS_WC
- Rsvd or Rs
## USB 3.0 Host Memory Map/Registers

### Host Registers

<table>
<thead>
<tr>
<th>Offset</th>
<th>Acronym</th>
<th>Description</th>
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<td>0x0420</td>
<td>PORTSC</td>
<td>Host Controller Port Register Set</td>
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<td>0x0424</td>
<td>PORTMSC</td>
<td>Rsvd: 11'hx</td>
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<td>0x0428</td>
<td>PORTU</td>
<td>Rsvd: 16'hx</td>
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<tr>
<td>0x042C</td>
<td>PORTLPUC</td>
<td>Rsvd: 32'hx</td>
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</table>

### Host Controller Runtime Registers

- **Rsvd: 18'hx**
- **Microframe Index**: Rsvd 32'hx

### Interrupter Registers

- **IMODC**: Rsvd: 30'hx
- **IMODI: 16'd4000**: Event Ring Segment Table Size: 16'b0
- **Event Ring Segment Table Base Address Register: 26'b0**
- **Event Ring Segment Table Base Address Register: 32'b0**
- **Event Ring Dequeue Pointer: 26'b0**
- **Event Ring Dequeue Pointer: 32'b0**

### Doorbell Register

- **DB Stream ID**
- **xHCI Extended Capabilities**: Rsvd: 8'hx
- **DB Target**

### USB Legacy Support Capability

- **USBLEGSUP**: m9, m8, m7
- **USBLEGCLSTS**: m6, m5, m4, m3, m2, m1, m0
- **xHCI Supported Protocol Capability (USB 2.0)**
- **MajorRevision: 8'h2**: MinorRevision: 8'h0
- **Name String: "USB"**: Next Capability Pointer
- **Rsvd: 27'hx**: Protocol Slot Type: 5'b0
Session Summary

• Discussed the differences between USB 3.0 and USB 2.0

• Described USB 3.0 Feature

• Presented Layered Protocol Architecture
  – Details on Protocol layer
  – Details on Link layer
  – Details on Physical layer

• Discussed USB 3.0 on LS1
  – Data structure and Memory map
For Further Information

• URLs
  - http://www.usb.org/developers/ssusb/

• Contact information
  – Jimmy Zhao, PE, System and Applications Engineering, DN
  – Jimmy.zhao@freescale.com
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