An Overview of the QorIQ T1040 Processor

FTF-NET-F0163

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Agenda

• Introduction
  - Block Diagram
  - Market Trend
• QorIQ T1040 processor features
  - Ethernet Switch
  - Serdes
  - Clocking
  - Power Management
• Collaterals
• Summary
QorIQ T1040 Processor

Processor
- 4x e5500, 64b, up to 1.4GHz
- Each with 256KB backside L2 cache
- 256KB Shared Platform Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory Subsystem
- 32/64b DDR3L/4 Controller up to 1600MHz

CoreNet Switch Fabric

High Speed Serial IO
- 4x PCIe Gen2 (5Gbps) Controllers
- 2x SATA 2.0, 3Gbps
- 2x USB 2.0 with PHY

Network IO
- FMan packet Parse/Classify/Distribute
- Lossless Flow Control, IEEE 1588
- Up to 4x 10/100/1000 Ethernet Controllers
- 8-Port Gigabit Ethernet Switch
- QUICC Engine
  - HDLC, 2x TDM

Green Energy Operation
- Fanless operation quad-core 1.4GHz
- Packet lossless deepsleep
  - Programmable wake-on-packet
  - Wake-on-timer/GPIO/USB/IRQ

Device
- 780-pin FC-PBGA package
- 23x23mm, 0.8mm pitch

Power targets
- Enable Convection cooled system design

Datapath Acceleration
- SEC- crypto acceleration
- PME- Reg-ex Pattern Matcher

Security Fuse Processor
- Security Monitor
- IFC
- Power Management
- eSDHC
- 2x DUART
- 2x I2C
- SPI, GPIO
- 2x USB 2.0 w/PHY
- DIU
QorIQ T1020 Processor

Processor
• 2x e5500, 64b, up to 1.4GHz
• Each with 256KB backside L2 cache
• 256KB Shared Platform Cache w/ECC
• Supports up to 64GB addressability (36 bit physical addressing)

Memory Subsystem
• 32/64b DDR3L/4 Controller up to 1600MHz

CoreNet Switch Fabric
High Speed Serial IO
• 4 PCIe Gen2 Controllers
• SATA 2.0, 3Gbps
• 2 USB 2.0 with PHY

Network IO
• FMan packet Parse/Classify/Distribute
• Lossless Flow Control, IEEE 1588
• Up to 4x 10/100/1000 Ethernet Controllers
• 8-Port Gigabit Ethernet Switch

• QUICC Engine
  • HDLC, 2x TDM

Green Energy Operation
• Fanless operation dual-core 1.4GHz
• Packet lossless deepsleep
  • Programmable wake-on-packet
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Device
• 780-pin FC-PBGA package
• 23x23mm, 0.8mm pitch

Power targets
• Enable Convection cooled system design

Datapath Acceleration
• SEC- crypto acceleration
• PME- Reg-ex Pattern Matcher

8-Lane 5GHz SERDES
QorIQ T1042 Processor

Processor
- 4x e5500, 64b, up to 1.4GHz
- Each with 256 KB backside L2 cache
- 256KB Shared Platform Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory Subsystem
- 32/64b DDR3L/4 Controller up to 1600MHz

CoreNet Switch Fabric

High Speed Serial IO
- 4 PCIe Gen2 Controllers
- SATA 2.0, 3Gbps
- 2 USB 2.0 with PHY

Network IO
- FMan packet Parse/Classify/Distribute
- Lossless Flow Control, IEEE 1588
- 5x 10/100/1000 Ethernet Controllers
- QUICC Engine
  - HDLC, 2x TDM

Green Energy Operation
- Fanless operation quad-core 1.4GHz
- Packet lossless deepsleep
  - Programmable wake-on-packet
  - Wake-on-timer/GPIO/USB/IRQ

Device
- 780-pin FC-PBGA package
- 23x23mm, 0.8mm pitch

Power targets
- Target Deep Sleep 150mW on special Part Numbers (1/2W AC System)

Datapath Acceleration
- SEC- crypto acceleration
- PME- Reg-ex Pattern Matcher

Security Fuse Processor
Security Monitor
IFC
Power Management
eSDHC
2x DUART
2x I2C
SPI, GPIO
2x USB 2.0 w/PHY
DIU
QorIQ T1022 Processor

Processor
- 2x e5500, 64b, up to 1.4GHz
- Each with 256 KB backside L2 cache
- 256KB Shared Platform Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory SubSystem
- 32/64b DDR3L/4 Controller up to 1600MHz

CoreNet Switch Fabric

High Speed Serial IO
- 4 PCIe Gen2 Controllers
- SATA 2.0, 3Gb/s
- 2 USB 2.0 with PHY

Network IO
- FMan packet Parse/Classify/Distribute
- Lossless Flow Control, IEEE 1588
- 5x 10/100/1000 Ethernet Controllers
- QUICC Engine
  - HDLC, 2x TDM

Green Energy Operation
- Fanless operation dual-core 1.4GHz
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Datapath Acceleration
- SEC- crypto acceleration
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Device
- 780-pin FC-PBGA package
- 23x23mm, 0.8mm pitch

Power targets
- Target Deep Sleep 150mW
- on special Part Numbers
  (1/2W AC System)
QorIQ T Series: One of the Industry’s Most Scalable, Pin-Compatible Communications Processor Family

- Dual-Core up to 1.4GHz
- Integrated GbE Switch

- Quad-Core up to 1.4GHz

- Eight Virtual Cores up to 1.8GHz

Scale from dual, quad to eight virtual cores with QorIQ T1/T2 devices
# Personality Comparison Chart

<table>
<thead>
<tr>
<th></th>
<th>P1020, P1011, P1021, P1012</th>
<th>P1022, P1013</th>
<th>T1020</th>
<th>T1022</th>
<th>T1040</th>
<th>T1042</th>
<th>T2081</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU</strong></td>
<td>1 to 2 x e500</td>
<td>1 to 2 x e500</td>
<td>2 x e5500</td>
<td>2 x e5500</td>
<td>4 x e5500</td>
<td>4 x e5500</td>
<td>4 x e6500/8 threads</td>
</tr>
<tr>
<td></td>
<td>Up to 800MHz</td>
<td>Up to 1200MHz</td>
<td>1200-1400MHz</td>
<td>1200-1400MHz</td>
<td>1200-1400MHz</td>
<td>1200-1400MHz</td>
<td>1500 - 1800MHz</td>
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<tr>
<td></td>
<td>32K I/D</td>
<td>32K I/D</td>
<td>32K I/D</td>
<td>32K I/D</td>
<td>32K I/D</td>
<td>32K I/D</td>
<td>32K I/D</td>
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<tr>
<td><strong>L2 Cache</strong></td>
<td>256KB</td>
<td>256KB</td>
<td>256KB/Core</td>
<td>256KB/Core</td>
<td>256KB/Core</td>
<td>256KB/Core</td>
<td>256KB/Core, 2MB shared</td>
</tr>
<tr>
<td><strong>Platform Cache</strong></td>
<td>256KB</td>
<td>256KB</td>
<td>256KB</td>
<td>256KB</td>
<td>256KB</td>
<td>256KB</td>
<td>512KB</td>
</tr>
<tr>
<td><strong>DDR I/F Type/Width</strong></td>
<td>DDR2/3</td>
<td>DDR2/3</td>
<td>DDR3L/4</td>
<td>DDR3L/4</td>
<td>DDR3L/4</td>
<td>DDR3L/4</td>
<td>DDR3/3L</td>
</tr>
<tr>
<td></td>
<td>16/32-bit, 800MHz</td>
<td>32/64-bit, 1600MT/s</td>
<td>32/64-bit, 1600MT/s</td>
<td>32/64-bit, 1600MT/s</td>
<td>32/64-bit, 1600MT/s</td>
<td>32/64-bit, 1600MT/s</td>
<td>32/64-bit, 2133MT/s</td>
</tr>
<tr>
<td><strong>10/100/1000 Ethernet (with IEEE1588v2)</strong></td>
<td>3 x 10/100/1000</td>
<td>2 x 10/100/1000</td>
<td>4 x 10/100/1000</td>
<td>2 x 2.5 + 5 x 10/100/1000</td>
<td>4 x 10/100/1000</td>
<td>2 x 2.5 + 5 x 10/100/1000</td>
<td>2 x 2.5/10G + 6x 1G</td>
</tr>
<tr>
<td><strong>Ethernet Switch</strong></td>
<td>--</td>
<td>--</td>
<td>8-Port GE Switch</td>
<td>No</td>
<td>8-Port GE Switch</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td><strong>TDM</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
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<tr>
<td><strong>QUICC Engine</strong></td>
<td>In P1021/12</td>
<td>No</td>
<td>TDM and HDLC</td>
<td>TDM and HDLC</td>
<td>TDM and HDLC</td>
<td>TDM and HDLC</td>
<td>No</td>
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<tr>
<td><strong>SERDES</strong></td>
<td>4 lanes</td>
<td>6 lanes</td>
<td>8 lanes(5GHz)</td>
<td>8 lanes(5GHz)</td>
<td>8 lanes(5GHz)</td>
<td>8 lanes(5GHz)</td>
<td>8 lanes(5GHz)</td>
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<td></td>
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<td></td>
<td>8 lanes(5GHz)</td>
<td>8 lanes(5GHz)</td>
<td>8 lanes(5GHz)</td>
<td>8 lanes(5GHz)</td>
<td>8 lanes(10GHz)</td>
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<tr>
<td><strong>PCI-Exp</strong></td>
<td>2 (Gen-1)</td>
<td>3 (Gen-1)</td>
<td>4 (Gen-2)</td>
<td>4 (Gen-2)</td>
<td>4 (Gen-2)</td>
<td>4 (Gen-2)</td>
<td>3 (Gen2) and 1 (Gen3)</td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td></td>
<td></td>
<td>Pin Compatible</td>
<td></td>
<td></td>
<td></td>
<td>Pin Compatible</td>
</tr>
</tbody>
</table>

*Note: The images, tables, and text are extracted from the document and formatted for better readability.*
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<th>T2081</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIU</td>
<td>--</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>SATA</td>
<td>2 controller</td>
<td>1.5 or 3Gbaud</td>
<td>2 controller</td>
<td>1.5 or 3Gbaud</td>
<td>2 controller</td>
<td>1.5 or 3Gbaud</td>
<td>No</td>
</tr>
<tr>
<td>USB2.0</td>
<td>2 ULPI controllers</td>
<td>2 with PHY</td>
<td>2 with PHY</td>
<td>2 with PHY</td>
<td>2 with PHY</td>
<td>2 with PHY</td>
<td>2 with PHY</td>
</tr>
<tr>
<td>Memory Card</td>
<td>SD/MMC</td>
<td>SD/MMC/SDXC</td>
<td>SD/MMC/SDXC</td>
<td>SD/MMC/SDXC</td>
<td>SD/MMC/SDXC</td>
<td>SD/MMC/SDXC</td>
<td>SD/MMC/SDXC</td>
</tr>
<tr>
<td>Accelerators</td>
<td>SEC3.3</td>
<td>SEC3.3</td>
<td>DPAA, PME SEC5.0 with Trust Architecture</td>
<td>DPAA, PME SEC5.0 with Trust Architecture</td>
<td>DPAA, PME SEC5.0 with Trust Architecture</td>
<td>DPAA, PME SEC5.0 with Trust Architecture</td>
<td>DPAA, PME DCE, SEC5.2 with Trust Architecture</td>
</tr>
<tr>
<td>Package</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Pin Compatible</td>
</tr>
</tbody>
</table>

**Personality Comparison Chart**
<table>
<thead>
<tr>
<th>Features</th>
<th>Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Scalable Performance</strong></td>
<td><strong>Future Proofing</strong></td>
</tr>
<tr>
<td>Pin compatible dual core to eight virtual cores</td>
<td>Upgrade to higher performance as needed</td>
</tr>
<tr>
<td></td>
<td>&gt;2x-4x the performance of existing P1 series</td>
</tr>
<tr>
<td><strong>Gigabit Ethernet Switch</strong></td>
<td><strong>Lowers System Cost/Simplifies design</strong></td>
</tr>
<tr>
<td>Integrated Gigabit Ethernet Switch</td>
<td>Eliminates cost of external GE switch</td>
</tr>
<tr>
<td></td>
<td>Simplifies HW and SW implementation</td>
</tr>
<tr>
<td></td>
<td>Reduces overall system power</td>
</tr>
<tr>
<td><strong>Accelerators</strong></td>
<td><strong>Enforce SLAs/Reduce CPU cycles</strong></td>
</tr>
<tr>
<td>DPAA - Classification, Traffic Management Pattern Matching Security</td>
<td>Manage traffic guarantees to enforce SLAs</td>
</tr>
<tr>
<td></td>
<td>Security policies based on application/services</td>
</tr>
<tr>
<td></td>
<td>High performance HW based encryption</td>
</tr>
<tr>
<td></td>
<td>VortiQa Security Appliance S/W and AppID</td>
</tr>
<tr>
<td><strong>Hardware Assisted Virtualization</strong></td>
<td><strong>Higher performance (Vs. software emulation)</strong></td>
</tr>
<tr>
<td>Hypervisor level</td>
<td>Enables virtualization layer to enforce system security</td>
</tr>
<tr>
<td>I/O MMU – controls memory I/Os can access</td>
<td>Simplifies I/O virtualization and sharing</td>
</tr>
<tr>
<td>Support for Topaz, KVM, Linux Containers,</td>
<td>Flexibility to use multiple options to meet system needs</td>
</tr>
<tr>
<td></td>
<td>Support for S/W Hypervisor, KVM and Linux Containers</td>
</tr>
<tr>
<td><strong>Power Management</strong></td>
<td><strong>Green Energy Efficient System Designs</strong></td>
</tr>
<tr>
<td>Best performance per watt</td>
<td>Optimized for best performance and power</td>
</tr>
<tr>
<td>Deep Sleep – proxy for sleeping hosts</td>
<td>Enables Compliance with Energy Consumption standards</td>
</tr>
<tr>
<td>Enables ½ Watt AC</td>
<td>(ECC, EnergyStar, ECMA 393)</td>
</tr>
<tr>
<td></td>
<td>Power Management software as part of SDK</td>
</tr>
</tbody>
</table>
QorIQ T1040 Software & Tools at a Glance

• Two Reference Design Boards
  - T1040RDB
  - T1042RDB
• Software Support
  - Yocto based SDK
  - SDK support includes
    ▪ Legacy features (refer SDK 1.4 release notes)
    ▪ New features
    ▪ FMAN and QE microcode
    ▪ Linux based QE drivers for TDM, UART and HDLC
• QorIQ Configuration Suite
• Code Warrior based debugger, flash programmer
QorIQ T1040RDB System
QorIQ T10xx Product Kit Options

**Integrated Gigabit Ethernet Switch And bundled 2x QUAD PHYs**

- **T1040 Quad-Core**
  - 8-Port GE Switch
  - QSGMII
- **F104 Quad PHY**
- **F104 Quad PHY**

- **T1020 Dual-Core**
  - 8-Port GE Switch
  - QSGMII
- **F104 Quad PHY**
- **F104 Quad PHY**

**Without Gigabit Switch**

- **T1042 Quad-Core**
- **T1022 Dual-Core**

**Integrated Gigabit Ethernet Switch And bundled 2x QUAD PHYs**

- **T1040 Quad-Core**
  - 8-Port GE Switch
  - QSGMII
- **F104 Quad PHY**
- **F104 Quad PHY**

- **T1020 Dual-Core**
  - 8-Port GE Switch
  - QSGMII
- **F104 Quad PHY**
- **F104 Quad PHY**

**Without Gigabit Switch**

- **T1042 Quad-Core**
- **T1022 Dual-Core**
## Pin Multiplexing

<table>
<thead>
<tr>
<th>SerDes 1</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
<td>C</td>
<td>D</td>
<td>E</td>
<td>F</td>
<td>G</td>
<td>H</td>
</tr>
<tr>
<td>PCIe1 (5/2.5)</td>
<td>PCIe2 (5/2.5)</td>
<td>qsp.s1-4</td>
<td>qsp.s5-8</td>
<td>PCIe3 (5/2.5)</td>
<td>PCIe4 (5/2.5)</td>
<td>SATA2 (3/1.5)</td>
<td>SATA1 (3/1.5)</td>
</tr>
<tr>
<td>sg.s3</td>
<td>sg.s1</td>
<td>sg.s2</td>
<td>sg.s6</td>
<td>sg.s4</td>
<td>sg.s5</td>
<td>sg.m2 1G/2.5G</td>
<td>sg.m1 1G/2.5G</td>
</tr>
<tr>
<td>sg.m3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>T1040</th>
</tr>
</thead>
<tbody>
<tr>
<td>MI</td>
</tr>
<tr>
<td>L1VDD</td>
</tr>
<tr>
<td>USB:PHY</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

- **O1VDD/OVDD (1.8V)**
- **L1VDD (3.3V/2.5V)**
- **LVDD (2.5V)**
- **DVDD (3.3V/2.5V)**

- **CVDD (3.3V/1.8V)**
- **EVDD (runtime switchable supply 1.8V / 3.3 V)**
- **G1VDD (1.35V / 1.2V)**

---

**Note:**
- **External Use**
- **15**
Agenda

• Introduction
  - Block Diagram
  - Market Trend

• **QorIQ T1040 processor features**
  - Ethernet Switch
  - Serdes
  - Clocking
  - Power Management

• Collaterals
• Conclusion
QorIQ T1040: Gigabit Ethernet Switch

- **Advanced Features**
  - Priority flow control - lossless
  - Lower latency and shared buffer management
  - Advanced classification, shaping and policing

- **Power savings**
  - With support for latest standards including IEEE 802.3az Energy Efficient Ethernet (EEE)

- **Cost savings**
  - Through switch integration, low-pin count QSGMII connectivity and port count / cost optimization

- **Increased ROI - Lower TTM and high re-use**
  - Integrated solution kit with software reuse potential

- **Support for Full featured L2 software stacks**
Ethernet Switch Interface with Frame Manager

- 8 L2-switch ports + 3 FMAN ports
- 2 ports of Ethernet switch is connected to FMAN and operating 2.5 Gbps (aggregating to 5 Gbps)

**OR**

- 8 L2-switch ports + 4 FMAN ports. 1 port of Ethernet switch is connected to FMAN @ 2.5 Gbps.

Control packets are queued on the Ethernet Switch CPU-register interface and can be accessed (receive and transmit) through any e5500 core. This space is memory mapped in T1040 (CCSR space).
QorIQ T104x SERDES

- QorIQ T104x device supports single 8 lane SerDes.

- There are two PLL’s in the SerDes.
  - PLL1 provides clocking for lanes A:H and Ethernet switch
  - PLL2 provides clocking for Lanes C:H

- QorIQ T104x device supports the following network protocols through SerDes
  - QSGMII (T1040, T1020 only)
  - 1000 Base-KX
  - SGMII 2.5G (T1042, T1022 only)
  - SGMII
QSGMII (Quad Serial Gigabit Media Independent Interface)

- The **QSGMII** is a method of combining four **SGMII** lines into a 5Gbit/s interface.
- **QSGMII** uses significantly fewer signal lines than four **SGMII** busses.
### QorIQ T1040/20 SerDes Lane Multiplexing

With Ethernet switch

<table>
<thead>
<tr>
<th>SRDS_PRTCL_S1 RCW[128:135]</th>
<th>Lane A</th>
<th>Lane B</th>
<th>Lane C</th>
<th>Lane D</th>
<th>Lane E</th>
<th>Lane F</th>
<th>Lane G</th>
<th>Lane H</th>
<th>Parallel Port Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>69</td>
<td>PCIe1 (5/2.5)</td>
<td>SGMII (m3)</td>
<td>QSGMII (s1-4)</td>
<td>QSGMII (s5-8)</td>
<td>PCIe2 (5/2.5)</td>
<td>PCIe3 (5/2.5)</td>
<td>SGMII (m4)</td>
<td>SATA1</td>
<td>RGMII (FMAN MAC#5) RGMII (FMAN MAC#2, MAC#5)</td>
</tr>
<tr>
<td>66</td>
<td>PCIe1 (5/2.5)</td>
<td>SGMII (m3)</td>
<td>QSGMII (s1-4)</td>
<td>QSGMII (s5-8)</td>
<td>PCIe2 (5/2.5)</td>
<td>PCIe3 (5/2.5)</td>
<td>PCIe4 (5/2.5)</td>
<td>SATA1</td>
<td>2 RGMII (FMAN MAC #4 &amp; #5)</td>
</tr>
<tr>
<td>67</td>
<td>PCIe1 (5/2.5)</td>
<td>SGMII (m3)</td>
<td>QSGMII (s1-4)</td>
<td>QSGMII (s5-8)</td>
<td>PCIe2 (5/2.5)</td>
<td>PCIe3 (5/2.5)</td>
<td>PCIe4 (5/2.5)</td>
<td>SGMI (m5)</td>
<td>1 RGMII (FMAN MAC #4)</td>
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<tr>
<td>60</td>
<td>PCIe1 (5/2.5)</td>
<td>SGMII (m3)</td>
<td>QSGMII (s1-4)</td>
<td>QSGMII (s5-8)</td>
<td>PCIe2 (5/2.5)</td>
<td></td>
<td></td>
<td></td>
<td>2 RGMII (FMAN MAC #4 &amp; #5)</td>
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<tr>
<td>8D</td>
<td>PCIe1 (5/2.5)</td>
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<td>SGMII (s2)</td>
<td>PCIe2 (5/2.5)</td>
<td>SGMII (s6)</td>
<td>SGMII (s4)</td>
<td>SGMII (s5)</td>
<td>2 RGMII (FMAN MAC #4 &amp; #5)</td>
</tr>
<tr>
<td>89</td>
<td>PCIe1 (5/2.5)</td>
<td>SGMII (s3)</td>
<td>SGMII (s1)</td>
<td>SGMII (s2)</td>
<td>PCIe2 (5/2.5)</td>
<td>PCIe3 (5/2.5)</td>
<td>SGMII (s4)</td>
<td>SATA1</td>
<td>2 RGMII (FMAN MAC #4 &amp; #5)</td>
</tr>
</tbody>
</table>

- Ethernet switch connects with FMAN using MAC#1 and/or MAC#2
- MAC#2 used as additional RGMII port if Ethernet switch connected through MAC#1 only
- MAC#1 and MAC#2 are 2.5G ports.

**LEGEND**

“mn” indicates MAC# from FMan
“sn” indicates MAC# from Ethernet switch
QorIQ T1042/22 SerDes Lane Multiplexing

Without Ethernet switch

<table>
<thead>
<tr>
<th>SRDS_PRTCL_S1</th>
<th>Lane A</th>
<th>Lane B</th>
<th>Lane C</th>
<th>Lane D</th>
<th>Lane E</th>
<th>Lane F</th>
<th>Lane G</th>
<th>Lane H</th>
<th>Parallel Port availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>86</td>
<td>PCIe1 (5/2.5)</td>
<td>SGMII (m3)</td>
<td>SGMII (m1)</td>
<td>SGMII (m2)</td>
<td>PCIe2 (5/2.5)</td>
<td>PCIe3 (5/2.5)</td>
<td>PCIe4 (5/2.5)</td>
<td>SATA1</td>
<td>2 RGMII (FMAN MAC #4 &amp; #5)</td>
</tr>
<tr>
<td>87</td>
<td>PCIe1 (5/2.5)</td>
<td>SGMII (m3)</td>
<td>SGMII (m1)</td>
<td>SGMII (m2)</td>
<td>PCIe2 (5/2.5)</td>
<td>PCIe3 (5/2.5)</td>
<td>PCIe4 (5/2.5)</td>
<td>SGMII (m5)</td>
<td>1 RGMII (FMAN MAC #4)</td>
</tr>
<tr>
<td>A7</td>
<td>PCIe1 (5/2.5)</td>
<td>SGMII (m3)</td>
<td>SGMII (m1) 2.5G</td>
<td>SGMII (m2) 2.5G</td>
<td>PCIe2 (5/2.5)</td>
<td>PCIe3 (5/2.5)</td>
<td>PCIe4 (5/2.5)</td>
<td>SGMII (m5)</td>
<td>1 RGMII (FMAN MAC #4)</td>
</tr>
<tr>
<td>AA</td>
<td>PCIe1 (5/2.5)</td>
<td>SGMII (m3)</td>
<td>SGMII (m1) 2.5G</td>
<td>SGMII (m2) 2.5G</td>
<td>PCIe2 (5/2.5)</td>
<td>PCIe3 (5/2.5)</td>
<td>SGMII (m4)</td>
<td>SGMII (m5)</td>
<td>0 RGMII</td>
</tr>
<tr>
<td>40</td>
<td>PCIe1 (5/2.5)</td>
<td>SGMII (m1)</td>
<td>SGMII (m2)</td>
<td></td>
<td>PCIe2 (5/2.5)</td>
<td></td>
<td></td>
<td></td>
<td>2 RGMII (FMAN MAC #4 &amp; #5)</td>
</tr>
<tr>
<td>06</td>
<td>PCIe1 (5/2.5)</td>
<td></td>
<td></td>
<td></td>
<td>PCIe2 (5/2.5)</td>
<td>PCIe3 (5/2.5)</td>
<td>PCIe4 (5/2.5)</td>
<td>SATA1</td>
<td>2 RGMII (FMAN MAC #4 &amp; #5)</td>
</tr>
<tr>
<td>08</td>
<td>PCIe1 (5/2.5)</td>
<td></td>
<td></td>
<td></td>
<td>PCIe2 (5/2.5)</td>
<td>PCIe3 (5/2.5)</td>
<td>SATA1</td>
<td>SATA1</td>
<td>2 RGMII (FMAN MAC #4 &amp; #5)</td>
</tr>
<tr>
<td>8F</td>
<td>PCIe1 (5/2.5)</td>
<td>SGMII (m3)</td>
<td>SGMII (m1) 2.5G</td>
<td>SGMII (m2) 2.5G</td>
<td></td>
<td>SGMII (m4)</td>
<td>SGMII (m5)</td>
<td></td>
<td>0 RGMII</td>
</tr>
<tr>
<td>85</td>
<td>PCIe1 (5/2.5)</td>
<td>SGMII (m3)</td>
<td>SGMII (m1)</td>
<td>SGMII (m2)</td>
<td>PCIe2 (5/2.5)</td>
<td>SGMII (m4)</td>
<td>SGMII (m5)</td>
<td></td>
<td>0 RGMII</td>
</tr>
<tr>
<td>A5</td>
<td>PCIe1 (5/2.5)</td>
<td>SGMII (m3)</td>
<td>SGMII (m1) 2.5G</td>
<td>SGMII (m2) 2.5G</td>
<td>PCIe2 (5/2.5)</td>
<td>SGMII (m4)</td>
<td>SGMII (m5)</td>
<td></td>
<td>0 RGMII</td>
</tr>
<tr>
<td>00</td>
<td>PCIe1 (5/2.5)</td>
<td></td>
<td></td>
<td></td>
<td>PCIe2 (5/2.5)</td>
<td></td>
<td></td>
<td></td>
<td>2 RGMII (FMAN MAC #4 &amp; #5)</td>
</tr>
</tbody>
</table>

**LEGEND**

“mn” indicates MAC# from FMan
Ethernet Parallel Interfaces on QorIQ T104x Processors

- 2x RGMII or 1x MII interface supported.
- MII/RGMII selection for EC1 via RCW[EC1] field.
- MAC2 or MAC4 selection for EC1 via RCW[MAC2_GMII_SEL] field
- RGMII interface enabled for EC2 via RCW[EC2] field.
USB PHY

- Supports Dual on-chip integrated USB PHY
- Supports USB 2.0
- Works on 24MHz clock (non spread spectrum) on the SOC’s USBCLK pin
- Can also work on an internal reference clock (system clock at 100MHz) which can be pre divided to obtain 20 MHz reference clock
• QorIQ T1040 has the same DIU programming model as QorIQ P1022 with the following differences

<table>
<thead>
<tr>
<th>Feature</th>
<th>P1022 DIU</th>
<th>T1040 DIU</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Interface</td>
<td>24 bit RGB</td>
<td>12 bit dual data rate RGB</td>
</tr>
<tr>
<td>Pin multiplexing</td>
<td>Multiplexed with eLBC</td>
<td>Multiplexed with QUICC Engine</td>
</tr>
<tr>
<td>Platform to pixel clock frequency ratio</td>
<td>≥ 3</td>
<td>≥ 4</td>
</tr>
<tr>
<td>Maximum pixel clock</td>
<td>133MHz</td>
<td>150MHz</td>
</tr>
</tbody>
</table>
eSDHC New Features

• Supports SDXC cards
  - Up to 2TB space
• Supports cards with UHS-I speed grade
  - Ultra high speed grade
    ▪ SDR12, SDR25, SDR50, SDR104, DDR50
  - UHS-I cards work on 1.8V signaling
    - On board dual voltage regulators are needed to support UHS-I cards because card initialization happens at 3.3V and regular operations happen at 1.8V
    - SD controller provides a signal to control the voltage regulator. The signal is controlled via SDHC_VS pin
• eMMC 4.5 support (HS200, DDR)
• All modes of SD3.0, eMMC 4.4 and eMMC4.5 are supported except 8 bit DDR for eMMC.
QorIQ T1040 DDR Controller Features

• Legacy Features:
  - Support for 32/64 bit DDR3L and DDR4 SDRAM with ECC
  - Chip-Select interleaving support
  - Support for unbuffered and registered DIMMs, single-ranked, dual-ranked, and quad-ranked DIMMs

• DDR4 Specific Features:
  - New JEDEC POD12 interface standard (1.2V)
  - Support for 4 bank groups
  - DBI (Data Bus Inversion) feature
  - Command Address (CA Parity)
  - CRC for data bus
  - CAL mode (CS to Command Address Latency)
  - Low power auto self-refresh
Core, PAMU, PME for QorIQ T1040 Processors

- QorIQ T1040 has 64-bit core with backside L2 cache of size 256KB
- e5500 Backside L2 cache can significantly improve performance
  - Much lower L2 latency
  - 36-bit physical address support

<table>
<thead>
<tr>
<th>Core</th>
<th>L2 Latency</th>
<th>Dhrystone DMIPS/MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>e500v2 (Frontside L2)</td>
<td>23 core cycles</td>
<td>2.4</td>
</tr>
<tr>
<td>e5500 (Backside L2)</td>
<td>12 core cycles</td>
<td>3.0</td>
</tr>
</tbody>
</table>

- Single PAMU catering to all the I/O’s (PAACT entries are 128)
- Pattern Matching engine (2.2) supports 16,384 patterns as compared to 32K pattern support in PME 2.0
QUICC Engine in QorIQ T1040 Processors

- Supports one uQE block
- 64MHz SYSCLK support for ProfiBUS
- Support for two TDM [TDMA, TDMB] and two UCC [UCC1, UCC3]
- Protocols:
  - HDLC, Transparent
  - Synchronous UART
  - ProfiBUS
  - TDM/SI
- UCC1 signals are multiplexed with TDMA signals
- UCC3 signals are multiplexed with TDMB signals
What is VID?

- VID is a specific method of selecting the optimum voltage-level to guarantee performance and power targets.

- QorIQ device contains fuse block registers defining required voltage level. This eFUSE definition is accessed through the Fuse Status Register (DCFG_FUSESR).

- Customer software will read the VID value from factory-set efuse values and configure regulator values appropriately.

- For T1040, the core VDD/VDDC value will range from 0.97V to 1.025V in 12.5mV steps

<table>
<thead>
<tr>
<th>Power Pins</th>
<th>Power Islands on T1040</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Switchable Core and Platform</td>
</tr>
<tr>
<td>VDDC</td>
<td>Always ON core and Platform Supply</td>
</tr>
<tr>
<td>USB_SVDD</td>
<td>USB supply</td>
</tr>
</tbody>
</table>

- Start up voltage: 1.025 ± 30mV
- During normal operation: VID ± 30mV
## QorIQ T1040 Clock Signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Function</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYSCLK</td>
<td>Single ended primary clock input</td>
<td>64MHz to 133MHz</td>
</tr>
<tr>
<td>DIFF_SYSCLK/</td>
<td>Differential primary clock input</td>
<td>100MHz</td>
</tr>
<tr>
<td>DIFF_SYSCLK_B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDRCLK</td>
<td>Reference clock for DDR controller</td>
<td>64MHz to 133MHz</td>
</tr>
<tr>
<td>USBCLK</td>
<td>Clock input to the USB PHY's</td>
<td>24MHz</td>
</tr>
<tr>
<td>SD1_REF_CLKn_P/</td>
<td>Clock input to High speed Serial interfaces</td>
<td>100MHz, 125MHz</td>
</tr>
<tr>
<td>SD1_REF_CLKn_N</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
“Single Oscillator Source ” clock Mode

SYSCLK (64-133.33MHz)

DIFF_SYSCLK/DIFF_SYSCLK_B 100MHz

1.0V

LVDS

MUX

On Board Oscillator (100MHz)
3 Differential Outputs

XTAL

POR CONFIG [cfg_eng_use0]

USB PHY PLL

Core PLL

Platform PLL

SERDES PLL1

SERDES PLL2

DDR PLL

DDR PHY

64 - 133.33 MHz DDRCLK

64 - 133.33 MHz DDRCLK

SYSTEM CLOCK

RCW[DDR_REFCLOCK_SEL]
Multiple reference clock mode (Legacy mode)

- DDRCLK: 64MHz - 133MHz Oscillator
- SYSCLK: 64MHz - 133MHz Oscillator
- USBCLK: 24MHz Oscillator
- PCIe Gen2 compliant Clock Generator & Buffer: 25MHz Osc

PLLs:
- DDR PLL
- Platform PLL
- Core PLL’s
- USB PHY PLL
- SERDES PLL1 (5GHz for PCIe, QSGMII, SGMII)
- SERDES PLL2 (3GHz for SATA, 3.125GHz for SGMII 2.5G)
QorIQ T1040 Power States

e5500 States: Run, Doze and Nap
Each core can independently support each state

<table>
<thead>
<tr>
<th>Core activity state</th>
<th>CPU State</th>
<th>Processor Clocks</th>
<th>Snoops Responded</th>
<th>Interrupts Responded</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>PH00</td>
<td>Run</td>
<td>On</td>
<td>Yes</td>
<td>Yes</td>
<td>Core clock adaption can be enabled</td>
</tr>
<tr>
<td>PH10</td>
<td>Doze</td>
<td>On</td>
<td>Yes</td>
<td>Yes</td>
<td>Core stops dispatching new instructions</td>
</tr>
<tr>
<td>PH15</td>
<td>Nap</td>
<td>Off (Except time base)</td>
<td>No</td>
<td>Yes</td>
<td>Flush data cache before entering</td>
</tr>
</tbody>
</table>
# QorIQ T1040 SoC Power Management States

## QorIQ T1040 Device (SoC) states: LPM10, LPM20, LPM35, Deep Sleep

<table>
<thead>
<tr>
<th>SOC RCPM state</th>
<th>Equivalent P1022 State</th>
<th>Device Clocks</th>
<th>ASLEEP Asserted</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPM10</td>
<td>---</td>
<td>On</td>
<td>No</td>
<td>Software configured variant of the ‘full ON’ state where some cores are placed in a lower power state</td>
</tr>
<tr>
<td>LPM20</td>
<td>Sleep</td>
<td>Cores in Nap, time base stopped</td>
<td>Yes</td>
<td>Only modules required for wakeup will have a running clock.</td>
</tr>
<tr>
<td>LPM35</td>
<td>Deep Sleep</td>
<td>Only the blocks in ON domain have clock running.</td>
<td>Yes</td>
<td>Only used for entry to deep sleep</td>
</tr>
<tr>
<td>Deep Sleep</td>
<td></td>
<td></td>
<td></td>
<td>Power is removed from a major portion of SOC</td>
</tr>
</tbody>
</table>
QorIQ T1040 Deep Sleep

• A major portion of the QorIQ T1040 processor is switched OFF including the cores and DDR Controller.
• Only the blocks needed to detect wakeup and sequence the chip out of deep sleep are ON.
• QorIQ T1040 responds to incoming wake-up events, from Ethernet interface, USB or GPIO interrupt, while consuming very little power.

- VDD is switchable supply
- VDDC is always ON
- USB and SEC block can optionally be in ON/OFF domain
Clocking in Deep sleep mode (check with Anju)

- Deep Sleep operation switches platform clock to system reference clock.
- Frame Manager is ON during Deep sleep for Auto response.
- Frame Manager is clocked with 2* 125MHz RGMII_GTXCLK from PHY.
- MII mode requires Frame Manager to be clocked with System clock.
QorIQ T1040 Deep Sleep

HW-SW Seq of QM/BM

Linux on e5500

User App

SNMP

DHCP

User App

User-space Kernel

Network Stack

NetBIOS

ARP

ND

IGMP

PCle Driver

Ethernet Driver

AR Control

AR Config API

Linux PM core

DPAA

QM / BM

FM Eth Port

Classifier

Auto-Response ucode

Kernel

DDRAM Memory

32/64-bit DDR3L/4 Memory Controller

256 KB Back side L2 Cache

Power Architecture® e5500

32 KB D-Cache

32 KB I-Cache

256KB Platform Cache

SFP

Security Monitor

16b IFC

PAMU

Peripheral Access Mgmt Unit

Sec 5.5 (XoR, CRC)

Queue Mgr.

PCD

2xDMA

QUICC Engine

Buffer Mgr.

8 Port

10Gbe Line

PM E 2.0

8-Lane 5GHz SERDES

DIU

SFP

Security Monitor

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2xDMA

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10Gbe Line

PM E 2.0

8-Lane 5GHz SERDES

DIU
QorIQ T1040 Deep Sleep Auto-response and wakeup

Linux on e5500

User App

SNMP

DHCP

User App

Network Stack

NetBIOS

ARP

ND

IGMP

PCIe Driver

AR Control

Ethernet Driver

AR Config API

Auto-Response ucode

User-space

Kernel

Linux PM core

FM Eth Port Classifier

DPAA

QM / BM

DIU

SFP

Security Monitor

16b IFC

Power Mgt

eSDHC

PCIe 2x DMAM

PCIe

8 Port

PCIe

PAMU

Peripheral Access Mgmt Unit

Power Architecture® e5500

256 KB Back side L2 Cache

32 KB D-Cache

32 KB I-Cache

256KB Platform Cache

32/64-bit DDR3L/4 Memory Controller

DDR Memory

CoreNet Coherency Fabric

Sec 5x (XOR, CRC)

Queue Mgr.

PCI

PCIE

PCIE

SATA 2.0

SATA 2.0

QUICC Engine

Debug

Watchpoint Cross Trigger

Perf Monitor

CoreNet Trace

8-Lane 5GHz SERDES

Session Request

Ping/ARP/IGMP Packet
Deep sleep related

- VDD and VDDC can be powered through separate regulators
- VDDC should ramp before/along with VDD
- Lossless mode supported for RGMII
- FMAN works on SYSCLK for MII mode and may not be lossless
- EVT_B2 aka power enable, should not be sampled when PORESET_B is asserted. There should be an on board pull up on this signal.
- USB and SEC block can optionally be switched ON/OFF in deep sleep, board level considerations required
- EPU and NPC resources are not available as Debug

SDHC related

- RCW loading from SD interface using voltage translators is not supported
 Agenda

• Introduction
  − Block Diagram
  − Market Trend
• QorIQ T1040 processor features
  − Ethernet Switch
  − Serdes
  − Clocking
  − Power Management
• **Collaterals**
• Conclusion
Collaterals / Documentation

• **On the Core:**
  - e5500 core Reference Manual (Rev4, 2013)

• **On the SoC device:**
  - QorIQ T104x Processor Fact-sheet and Product brief
  - HW Spec Rev D
  - Reference Manual Rev B
  - QEIWRM
  - Errata-sheet Rev A
  - Application Notes
    - AN4773 - Migration Guide from T2081 to T1040
Agenda

• Introduction
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  – Power Management
• Collaterals
• Summary
QorIQ T1 and T2 Families Extend Market Leadership

• First 64-bit embedded processor with an integrated GbE switch
  – Reduces system cost, design complexity and power

• One of the industry’s most scalable, pin-compatible family of devices
  – Performance scalability with a common architecture

• Energy efficiency and low power
  – Designed to be compliant to European Code of Conduct, and EnergyStar energy consumption standards

• Ideal for low-to mid-range networking and industrial connectivity applications
Freescale’s Comprehensive Ecosystem

### Tools and Operating Systems
- CodeWarrior
- CriticalBlue
- ENEA
- Green Hills Software
- QNX
- Mentor Embedded
- Wind River
- Wind River

### Virtualization
- KVM
- lx Containers

### Application Software
- VortiQa
- Elliptic
- SWIND
- Bitdefender
- Broadweb
- One Convergence
- Mocana

### Systems Integration & Services
- RadiSys
- Mercury Computer Systems
- Advantech
- Portwell
- Lanner
- Emerson
- Flextronics

### Development Systems
- NXP
- Freescale
- External Use | 45
Introducing The QorIQ LS2 Family

Breakthrough, software-defined approach to advance the world’s new virtualized networks

New, high-performance architecture built with ease-of-use in mind
Groundbreaking, flexible architecture that abstracts hardware complexity and enables customers to focus their resources on innovation at the application level

Optimized for software-defined networking applications
Balanced integration of CPU performance with network I/O and C-programmable datapath acceleration that is right-sized (power/performance/cost) to deliver advanced SoC technology for the SDN era

Extending the industry’s broadest portfolio of 64-bit multicore SoCs
Built on the ARM® Cortex®-A57 architecture with integrated L2 switch enabling interconnect and peripherals to provide a complete system-on-chip solution
QorIQ LS2 Family

Key Features

- **High performance cores with leading interconnect and memory bandwidth**
  - 8x ARM Cortex-A57 cores, 2.0GHz, 4MB L2 cache, w Neon SIMD
  - 1MB L3 platform cache w/ECC
  - 2x 64b DDR4 up to 2.4GT/s

- **A high performance datapath designed with software developers in mind**
  - New datapath hardware and abstracted acceleration that is called via standard Linux objects
  - 40 Gbps Packet processing performance with 20Gbps acceleration (crypto, Pattern Match/RegEx, Data Compression)
  - Management complex provides all init/setup/teardown tasks

- **Leading network I/O integration**
  - 8x1/10GbE + 8x1G, MACSec on up to 4x 1/10GbE
  - Integrated L2 switching capability for cost savings
  - 4 PCIe Gen3 controllers, 1 with SR-IOV support
  - 2 x SATA 3.0, 2 x USB 3.0 with PHY

Unprecedented performance and ease of use for smarter, more capable networks
See the LS2 Family First in the Tech Lab!

4 new demos built on QorIQ LS2 processors:

- Performance Analysis Made Easy
- Leave the Packet Processing To Us
- Combining Ease of Use with Performance
- Tools for Every Step of Your Design