QorIQ Multicore Power Management, Optimize Power to the Actual usage

FTF-NET-F0443

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M A Y . 2 0 1 4
Session Abstract (Content & Objectives)

**Energy saving** has always been a major concern in end applications like consumer appliances, printers, etc ... It is now also becoming a strong requirement in infrastructure equipments to reduce energy costs and to comply with environmental constraints.

This session will present the various and innovative power management hardware features integrated in the latest *QorIQ 45nm and 28nm Multicore SoC’s* which allow system designers to save both static and dynamic power according to the actual usage done from the available features.

How to implement the power management features at Software/Linux level will be discussed in another complementary session, FTF-NET-F0035.

This presentation is not specification .. for precise implementation of a specific family and derivative, please go to the spec
• Power Management: Background and Use cases
  • QorIQ Multicore 45 nm Power Management Features
    (P3/P4/P5/P204x)
  • QorIQ Multicore 28 nm Power Management Features
    (T4/T2, T1, Qonverge B4)
• Other Considerations
Power Management Strategy – Top/Down Approach

• **Static Power-to-Usecase optimization**: Coarse-grain management through enabling/disabling used/unused blocks and optimizing max frequency

• **Economy mode (eg. night Vs day)**: during long period of no- or low- activity, put the system in “low power” or “sleep” mode waiting for activity to come back in service

• **Run-time Power optimization**: Fine grain dynamic power optimization during ”transient” (short) period of lower activity
Power Consumption - Background

• Power = Dynamic + Static

\[
\text{Power} = \text{Capacitance} \times \text{Frequency} \times \text{Voltage}^2 + \text{Current}_c x \text{Voltage}
\]

• Dynamic power is related to the activity performed and mainly due to:
  - Charging/discharging capacitor load
  - Dynamic hazards – switching glitches
  - Short-circuit currents
Can be reduced thru frequency adaption and clock gating

• Static power is not activity related and mainly due to:
  - Drain leakage
  - Junction leakage
  - Gate leakage
Can be reduced thru voltage adaption and power gating
QorIQ Multicore Power Management Features – In a glance

- Optimize Power spec through some “smart” and transparent dynamic frequency & voltage management techniques in the various IP blocks
- Statically optimize power per use-case by disabling completely unused functions / IPs
- Optimize core utilization Vs power thru SW-controlled frequency scaling when core(s) in reduced activity but still active
- Optimize core utilization Vs power thru some various low-power activity states when core(s) inactive or when SW enters idle task
- Optimize device (SoC) utilization Vs power thru deep sleep state when full device inactive
- Provide thermal sensing assistance
Agenda

• Power Management: Background and Use cases

• QorIQ Multicore 45 nm Power Management features (P3/P4/P5/P204x)

• QorIQ Multicore 28 nm Power Management features (T4/T2, T1, Qonverge B4)

• Other Considerations
QorIQ Multicore P-series (P3/P4/P5/P204x)

Example: P4080

P4080
P4080 – review Core Power Spec

*Looking at where Power is consumed…*

<table>
<thead>
<tr>
<th>Power Mode</th>
<th>Core Freq (MHz)</th>
<th>Plat Freq (MHz)</th>
<th>DDR Data Rate (MHz)</th>
<th>PME/FM Freq (MHz)</th>
<th>$V_{DD,CA}$, $V_{DD,CB}$, $V_{DD,PL}$, $SVDD$ (V)</th>
<th>Junction Temperature (°C)</th>
<th>Core and Platform Power$^{1}$ (W)</th>
<th>$V_{DD,PL}$ Power$^{2}$ (W)</th>
<th>$V_{DD,CA}$ Power$^{3}$ (W)</th>
<th>$V_{DD,CB}$ Power$^{3}$ (W)</th>
<th>$SVDD$ Power$^{6}$ (W)</th>
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<td>1000</td>
<td>600</td>
<td>1000</td>
<td>350</td>
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<td>13</td>
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<td>2, 3</td>
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<td>20.4</td>
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<tr>
<td>Maximum</td>
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<td>22</td>
<td>12.5</td>
<td>5.7</td>
<td>5.7</td>
<td>1.7</td>
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<td>533</td>
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<td>5</td>
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<tr>
<td>Maximum</td>
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<td>30</td>
<td>16.6</td>
<td>7.8</td>
<td>7.8</td>
<td>1.7</td>
<td>—</td>
<td>4</td>
</tr>
</tbody>
</table>

**Note:**
1. Combined power of $V_{DD,PL}$, $V_{DD,CA}$, $V_{DD,CB}$, $SVDD$ at 1.0 V with both DDR controllers and all SerDes banks active. Does not include I/O power.
2. Multicore activity factor of 0.7 relative to Dhrystone and 0.4 platform activity factor.
3. Typical power based on nominal processed device.
4. Maximum power with Dhrystone executing at 100% on all eight cores and executing DMA on the platform.
5. Thermal power assumes multicore activity factor of 0.7 relative to Dhrystone and executing DMA on the platform.
6. Maximum power provided for power supply design sizing.
Dynamic Frequency Adaption Capabilities – Example: P4080

• The four PLL’s can be programmed to independent frequencies
• Each CPU core can be individually configured, optimizing both the performance and power for the given application requirements
• Each CPU core input frequency can be changed “on the fly” via software control

For more details see SoC device Reference Manual
Core Power State (or Activity State)

- e500mc/e5500 States: **Run, Wait, Doze and Nap**
- Each core can independently support each state
- P4080 Device (SoC) states: **Run and Sleep**

### Processor Clocks | Snoops Responded To | Interrupts Responded To | Comments
---|---|---|---
On | Yes | Yes | Transparent Dynamic Power Management thru Clock Gating
On | Yes | Yes | Core stops dispatching new instructions
Off except time base | No | Yes | SW must flush & invalidate data cache before entering
Off (incl. time base) | No | Yes | All cores in NAP state IP blocks are halted and clocks gated off

**Note:** Unlike previous single-core Power and PowerQUICC families, in QorIQ multicore SoCs, power is managed thru **SoC level registers** accessible in **CCSR** from any core (described in RCPM section of each device Ref. Manual), this includes Cores State Management.
Core Doze/Nap States - details

On **DOZE** (and **WAIT**):

- Because state is retained in the caches and core registers, and the caches continue to participate in snooping activities, software does not need to perform any specific actions prior to entering the *doze* state to ensure that coherent state is maintained.

On **NAP**:

- Since the caches no longer continue to participate in snooping activities, software should always flush, then invalidate the caches prior to initiating *nap* state to ensure that any modified data is written out to backing store.

- Upon exit from *nap* state, software must update any TLB entries that may have changed due to invalidations that were missed while the core was stopped. In general, this will require the flushing of any dynamic TLB entries and reloading them from the software page table.

- Because the core must flush its caches immediately prior to entering the *nap* state, the *nap* state will generally only be initiated by writing the appropriate integrated device registers by the specific core which will enter the *nap* state (that is, a core will generally nap itself, not another core).

**Cost and Saving:**

- For ballpark estimation (depends on frequency, temp, load …), rough estimate of *Doze* power is in the range of 70-80% of *Active (Run)* power, 40-50% for *Nap*

- Wake-up delay from external Interrupt to executing first instruction is in the 50-100 core cycles for both *Doze* and *Nap*. Recovering from *Nap* requires more overhead due to L1-cache invalidation.
Disabling Unused IP Blocks -- Example: P4080

SoC device level registers (in CCSR) for controlling IP blocks global Clock Gating

Disabling an IP thru these registers should be done once after PORESET and does not allow reenabling until next PORESET.
QorIQ P4/P3/P5/P204x Multicore Power Management – a Summary

- **Some dynamic and transparent power optimization techniques:**
  - Fine-grained clock gating is used throughout the CPU core and SoC platform. If a circuit is unused/idle during a particular clock cycle, its clock is disabled in order to reduce the dynamic power.

- **Dynamic SW control over cores operating frequencies:**
  - Several PLLs for feeding cores (four in P4, two in P5), each core clock can be sourced from one over several of these PLLs and with in addition an optional /2 division factor.
  - Software can switch each Core source PLL and frequency divider glitchlessly and nearly instantaneously.

- **Dynamic SW control over reduced power modes:**
  - Core-level reduced power modes:
    - core Doze (stop execution, accessible thru SoC register or WAIT instruction)
    - core Nap (clocks stopped, no snooping)
  - Device-level reduced power mode sleep (clock stopped for all IPs)

- **Static SW control over unused IPs power:**
  - Unused blocks can be disabled (clock gating) through software configuration, saving the dynamic power associated with each functional block (PCIe, SRIO, DDR-ctrlr, SerDes …)
  - Once a block has been disabled thru SoC registers, it can only be re-enabled through system PORESET

- **Note:** in P-series 45nm no support for:
  1) Dynamic forced Volt/Frequency Scaling (DVFS)
  2) Voltage scaling
  3) Voltage gating
Thermal Monitoring support

**P-serie/T-serie provides on-chip sensor diode(s)**

- allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system

- Two pins (Tem_anode, Temp_cathode) may be connected to a temperature diode monitoring device (sensor) such as the Analog Devices, ADT7461A™. Such device uses the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the processor and its environment.

- **P4080 HW-spec** of the chip’s on-board temperature diode:
  - Operating range: 10 – 230µA
  - Ideality factor over 13.5 – 220 µA: \( n = 1.007 \pm 0.008 \)

- Guidelines on implementing Temp. Measurement System and calibration process, see App-Notes **AN2929 & AN4787**
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- Other Considerations
QorIQ Multicore T-series – T1

T1040 / T1042 / T1020 / T1022:
- two or four e5500 32/64b cores with private L1/L2 caches
- with or without 8-port L2-Switch
QorIQ Multicore T-serie – T2/T4

**T4240**:
- 3 Clusters
- 12 Cores
- 24 Threads

**T4240**:
- Three cluster 12xcore/24xthread e6500 32/64b w/ Altivec , three DDR controllers

**T4160**:
- Two clusters 8xcore/16xthread e6500 32/64b w/ Altivec , two DDR controllers

**T2080/2081**:
- One cluster 4xcore/8xthread e6500 32/64b w/ Altivec , one DDR controllers
T Series 28nm Power Management - Summary

• All T-series support:
  – Disabling of unused IPs (providing complete clock gating)
  – Core clock frequency adaption controlled by SW (thru several configurable PLLs and division factors)
  – Power Architecture reduced power states (Core Doze/Nap, Device Sleep)
  – Internal thermal sensor

• In addition in T2 and T4:
  – **Power Gating with State Retention** technology to reduce Static Power in addition to Dynamic Power
  – available at different levels: Core, Cluster, Device, Altivec
  – **Note**: applies also to QorIQ Qonverge B4 family

• In addition in T1:
  – Supports **Deep Sleep** device level state
Power Gating with State-Retention - Principle

Each flip-flop can save its state locally, no need to clock out to external memory. Additional power rail ensures that state is kept while logic is powered off.

Very fast on/off switching ~100 cycles.

Technology is brought in after successful usage at other Freescale division.

Note: This is just one implementation
e6500 Core Power Management States (or Activity States)

For more details see e6500 Core Reference Manual

- PW10 (Drowsy) Core
  - Wait instruction
  - Both threads must be in PW10
  - Clocks stopped and power gated
  - Core state retained except L1-caches
  - L1 D-Cache HW-invalidated
  - L1 I-Cache HW-invalidation configurable
  - No snoop w/ core clocks being turned off
  - Resumable on stash, Interrupt, reservation cleared
  - Similar in power saving as PH20

- PH00 (RUN) Core
  - Thread suspends instructions
  - Clocks kept on
  - Core enters PH10 when both threads have signaled entering PH10

- PH10 (DOZE) Core
  - Clocks kept on
  - Core enters PH10 when both threads have signaled entering PH10

- PH15 (NAP) Core
  - Clocks stopped except TimeBase
  - Core state retained
  - No snoop on L1, caches must be flushed
  - Resumable

- PH20 (Drowsy) Core
  - Power Gated w/ state retained
  - State and resume similar to NAP
  - Lower power, longer latency Vs PH15

- PH30 (OFF) Core
  - Core power & clock gated, no state retained
  - Not resumable (requires core reset)
T4/T2 Cluster and Device states

**Cluster**

- **PCL00** (default)
  - Full-On

- **PCL10** (Drowsy cluster)
  - All cores should be put in PH20 prior to entering PCL10
  - Clocks and power gated with state retained
  - L2 no longer snoops
    (must be flushed & invalidated before by SW)
  - Resumable from interrupt

**SoC**

- **LPM10**
  - At least one core not in PH00
  - Implicit mode, no configuration

- **LPM20** (Device sleep)
  - Device sleep
  - All cores in PH20, cluster in PCL10
  - Clocks and Power gated
  - Platform and all IP clocks off
  - Core Timebase off
  - Resumable
# e6500 Power States - saving and wake-up time compare

<table>
<thead>
<tr>
<th>Cluster State</th>
<th>PCL00</th>
<th>PCL00</th>
<th>PCL00</th>
<th>PCL00</th>
<th>PCL00</th>
<th>PCL10</th>
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<tbody>
<tr>
<td>Core State</td>
<td>PH00</td>
<td>PH10/PW10</td>
<td>PH15</td>
<td>PW20</td>
<td>PH20</td>
<td>PH20</td>
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<tr>
<td>Cluster Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Core Voltage</td>
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<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Cluster Clock</td>
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<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Off</td>
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<tr>
<td>Core Clock</td>
<td>On</td>
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<td>Off</td>
<td>Off</td>
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<td>L2 Cache</td>
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<td>SW Flushed</td>
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<td>HW Invalidated</td>
<td>SW Invalidated</td>
<td>SW Invalidated</td>
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<td>Wakeup Time</td>
<td>Active</td>
<td>Immediate</td>
<td>&lt; 30 ns</td>
<td>&lt; 200 ns</td>
<td>&lt; 600 ns</td>
<td>&lt; 1us</td>
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<td></td>
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</table>
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Advanced Power and Energy Management - Summary

Matching consumption to load

Tiered APM Hierarchy

- Core
  - Altivec
    - T
    - T
  - e6500
    - 32K
    - 32K
- Run, Doze, Nap
- Wait
- Power Gating (state retention)
- AltiVec low power
- Dynamic clock gating

SoC

- 2048KB Banked L2
- Run, Nap
- Dynamic frequency switching
- Power Gating (state retention)
- Dynamic clock gating

Clusters

- CoreNet
- Cache
- DDR
- DPAA
- FMAN
- QMAN
- SoC sleep with state retention
- Cascade power management
- Low-power DDR-ctrlr / self refresh
- Dynamic clock gating
- Energy Efficient Ethernet (EEE)
Power Management SW Support - Topics

• Static disabling of unused functions and IP’s
  – through BSP config

• CPU idle
  – Kernel Idle task to make use of cores low-power states (e500) and WAIT instruction (e500mc)

• Scaling CPU capacity
  – By removing/plugging a CPU (eg. Linux CPU Hotplug)
  – By scaling down/up CPU frequencies

• System Suspend
  – Put system into low power states on user command
  – Making use of SoC device Sleep state

• … covered in FTF-NET-F0035 session
Summary

- QorIQ P and T series provide a whole set of Power Management features to help optimize **Power Consumption and Thermal requirements according to the actual usage.**
  - Frequency adaption
  - Clock Gating
  - Core, Cluster and Device activity states
- T series (T2/T4) introduces enhancements thru **Power Gating with State Retention** at core, cluster and device levels
Backups
Introducing The QorIQ LS2 Family

Breakthrough, software-defined approach to advance the world’s new virtualized networks

**New, high-performance architecture built with ease-of-use in mind**
Groundbreaking, flexible architecture that abstracts hardware complexity and enables customers to focus their resources on innovation at the application level

**Optimized for software-defined networking applications**
Balanced integration of CPU performance with network I/O and C-programmable datapath acceleration that is right-sized (power/performance/cost) to deliver advanced SoC technology for the SDN era

**Extending the industry’s broadest portfolio of 64-bit multicore SoCs**
Built on the ARM® Cortex®-A57 architecture with integrated L2 switch enabling interconnect and peripherals to provide a complete system-on-chip solution
QorIQ LS2 Family
Key Features

High performance cores with leading interconnect and memory bandwidth
- 8x ARM Cortex-A57 cores, 2.0GHz, 4MB L2 cache, w Neon SIMD
- 1MB L3 platform cache w/ECC
- 2x 64b DDR4 up to 2.4GT/s

A high performance datapath designed with software developers in mind
- New datapath hardware and abstracted acceleration that is called via standard Linux objects
- 40 Gbps Packet processing performance with 20Gbps acceleration (crypto, Pattern Match/RegEx, Data Compression)
- Management complex provides all init/setup/teardown tasks

Leading network I/O integration
- 8x1/10GbE + 8x1G, MACSec on up to 4x 1/10GbE
- Integrated L2 switching capability for cost savings
- 4 PCIe Gen3 controllers, 1 with SR-IOV support
- 2 x SATA 3.0, 2 x USB 3.0 with PHY

Unprecedented performance and ease of use for smarter, more capable networks

SDN/NFV Switching

Data Center

Wireless Access
See the LS2 Family First in the Tech Lab!

4 new demos built on QorIQ LS2 processors:

- Performance Analysis Made Easy
- Leave the Packet Processing To Us
- Combining Ease of Use with Performance
- Tools for Every Step of Your Design
# P4080 – review I/O Power

*Looking at where Power is consumed …*

Here are IO power estimates from P4080 Hardware spec.

<table>
<thead>
<tr>
<th>Interface</th>
<th>Parameter</th>
<th>Symbol</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
<th>Notes</th>
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<td>DDR3 64 bits per controller</td>
<td>667 MHz data rate</td>
<td>GVD (1.5 V)</td>
<td>0.733</td>
<td>1.803</td>
<td>W</td>
<td>1, 2, 5, 6</td>
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<td>1000 MHz data rate</td>
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<td>0.806</td>
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<td>1200 MHz data rate</td>
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<td></td>
<td>1299 MHz data rate</td>
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<td>0.964</td>
<td>2.127</td>
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<td>HSSI: PCI-e, SGMII, SATA, SRIO, Aurora, Debug, XAUJ</td>
<td>x1, 1.25 G-baud</td>
<td>XVD (1.5 V)</td>
<td>0.078</td>
<td>0.087</td>
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<tr>
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<th>Unit</th>
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**Note:**
1. The typical values are estimates and based on simulations at 65 °C.
2. Typical DDR power numbers are based on one 2-rank DIMM with 40% utilization.
3. Assuming 15 pF total capacitance load
4. GPIOs are supported on 1.8 V, 2.5 V, and 3.3 V rails.
5. Maximum DDR power numbers are based on one 2-rank DIMM with 100% utilization.
6. The maximum values are estimated and they are based on simulations at 105 °C. The values are not intended to be used as the maximum guaranteed current.
P4080 Power Management Programming Model (cont’d)

Other SoC device level registers (in CCSR) to manage Power

SRDSBnRSTCTL
(SerDes Bank n Reset Control Register)

SerDes power down: shuts down the PLL, all of the receiver amplifiers, all of the samplers and places the transmitters in 3-state.

BnGCRm0
(Bank n General Control Register 0 – Lane m)
Altivec Power Management

- Altivec is e6500 core SIMD vector unit, including internal 128b vector registers and several execution units.
- Single Altivec unit per core shared by the two threads
- Each core’s Altivec unit can be placed into low power with state retention thru a clock & power gating mode.
- Altivec low-power state can be SW controlled (thru CDSR0 core’s register) and/or automatically HW controlled based on dynamic need

For details see e6500 Core Reference Manual
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