Simulation of Packaged Component Electrical Performance

FTF-SDS-F0024

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**Session Introduction**

- **Electrical Simulation of Package and Assembly**
  - The integrated circuit package is a crucial element in overall system performance.
  - Power and signal integrity within the package are essential for robust system performance.
  - Freescale conducts extensive electrical simulation of the package and assembly design to assure the performance of Freescale products.
  - This presentation will provide an overview of aspects of this modeling and simulation for automotive and microcontroller packages.

- **Presentation by Neil Tracht – Manager, Wirebond Package Design & Electrical Simulation**
Session Objectives

• After completing this session you will be able to:
  – Describe methods for package parasitic extraction
  – Name the types of electrical analysis preformed on IC packages
  – Describe how the electrical performance of the IC package impacts system performance
  – Describe how package parasitics are incorporated into Input Output Buffer Information Specification (IBIS) Models
Agenda

• Package analysis tools
• Power and signal integrity
  − PI/SI background
  − Power supply noise example
  − Signal integrity example
• Package design considerations
  − Substrate
  − Leadframe
  − Wire diameter and wire material
  − Current capacity
• Input Output Buffer Information Specification (IBIS) models
Package Analysis Tools
Package Electrical Analysis Tools

- Freescale uses a variety of 3D solvers to extract and model integrated circuit packages
- Full Package Analysis
  - Sigrity Power SI
  - Nimbic nWave
- Partial Package Analysis
  - Ansys HFSS and Q3D
  - Computer Simulation Technology (CST) Microwave Studio
Types of Packages

- Leadframe
  - QFP
  - QFN

- Substrate
  - BGA
  - LGA
  - 2-Layer and 4-Layer
  - SiP

- Redistributed Chip Package (RCP)
  - BGA
  - LGA
  - SiP
Understanding Package Parasitics
Package Parasitics

- **Resistance (R)**
  - Resistance in package conductors will create a voltage drop
  
  \[ V = IR \]
  
  - The DC resistance of a rectangular conductor is given by
  
  \[ R_{DC} = \frac{\rho \cdot \text{len}}{w \cdot t} \]
  
  - \( \rho \) is the bulk resistivity of the conductor
  - \( w \) is the width
  - \( t \) is the thickness
  - \( \text{len} \) is the length

- **AC Resistance**
  - Governed by “Skin Effect”
  - Skin Effect causes the current to crowd to the conductor surface
  - Depth is a function of square root of frequency
Package Parasitics

- Capacitance
  - Capacitance exists between any 2 conductors
  - The “self” capacitance - defined as the capacitance between a lead and a chosen reference conductor with no other conductors present
  - The “mutual” capacitance between 2 leads - the capacitance between the 2 leads with no other conductors present
Package Parasitics

- **Inductance**
  - Inductance will cause a voltage drop

\[ V = L \frac{dI}{dt} \]

- Self Inductance is the inductance of an individual loop
- Nearby loops have a mutual inductance
- Voltage over a loop depends on current in all loops

\[ V_1 = \frac{d}{dt} \left( L_1 I_1 + L_{12} I_2 + L_{13} I_3 + L_{14} I_4 \right) \]

- **Self Inductance**
- **Mutual Inductance**
Package Design Considerations
Design Considerations

• Substrate Package Design Considerations
  - Identify the critical signal nets and critical electrical specifications
  - Ball Map Plan package ball locations for critical electrical specifications
  - Supply network
    ▪ Minimize the power and ground network inductance and resistance
  - Critical signals
    ▪ Minimize the inductance and resistance for the critical signal nets
    ▪ Differential pairs
      • Differential pairs should be optimized for routing
      • Balance/ de-skew the differential pairs, data lanes
    ▪ Signals requiring isolation
      • Avoid switching nets adjacent to data lanes
      • Shield the critical signal nets with ground net
Design Considerations

• Substrate Package Design Considerations
  - Route VSS as a shield for the critical signal nets

Critical net VSS net
Design Considerations

- Substrate Package Design Considerations
  - DDR nets/differential nets balanced for electrical performance
Design Considerations

- Substrate Package Design Considerations
  - Continuous grounding is critical for high speed nets
  - Typical 4-Layer Package
    - Metal 1 – Signal Routing
    - Metal 2 – Ground
    - Metal 3 – Supplies
    - Metal 4 – BGA Pads and minimal routing
  - Critical nets should not route across breaks in the ground layer
Optimizing Power Integrity
Power Integrity

• VDD_LV - Time-Domain Voltage Waveform
  - Core noise is 78.52mV
  - Core noise is 6.54%
  - Above the +/-6% noise spec

Noise in mV and %

<table>
<thead>
<tr>
<th>Net</th>
<th>Noise, mV (overshoot/undershoot)</th>
<th>Noise % (overshoot/undershoot)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD_LV</td>
<td>42.51/-78.52</td>
<td>3.54/-6.54</td>
</tr>
</tbody>
</table>
Power Integrity

- VDD_LV - Time-Domain Voltage Waveform
  - Possible Solutions
    - Reduced Power Step
      - Core noise is 70.52mV
      - Core noise is 5.88%
    - On die bypass capacitance
      - Core noise is 70.86mV
      - Core noise is 5.90%
    - Solutions with the +/-6% noise spec
Wire Diameter

• Bond wire diameter is set by two limiting factors
  – Current capacity of the bond wire
    ▪ Limited by self-heating of the wire – a function of wire length and current
  – Voltage drop of package supply network
    ▪ Limited by supply noise margins

• Comparison of 18 um and 23 um diameter wire
  – Current Capacity
    ▪ Highest current die pad with longest bond wire identified
      • Required current - 38.04mA VDD supply
      • Current capacity of 23 um wire – 249.8mA
      • Current capacity of 18 um wire – 151.1mA

  ▪ Smaller diameter wire will meet current capacity requirements
Wire Diameter

- Comparison of 18 μm and 23 μm diameter wire
  - Voltage supply margin
    - Smaller diameter wire reduces supply margin by ~3.4mV
    - Supply budget is ±6% or ±90mV leaving ~34.5mV of margin
    - Smaller diameter wire meets supply margin requirements

<table>
<thead>
<tr>
<th>Wire Diameter</th>
<th>Overshoot/Undershoot mV</th>
<th>Overshoot/Undershoot percent</th>
</tr>
</thead>
<tbody>
<tr>
<td>23μm</td>
<td>0.11/-52.11</td>
<td>0.01/-3.47</td>
</tr>
<tr>
<td>18μm</td>
<td>-3.94/-55.47</td>
<td>-0.26/-3.70</td>
</tr>
</tbody>
</table>
Leadframe Design

- QFP Power Bar Design
  - Options to connect power bar
    - Fixed lead versus jumper wires
    - Jumper wires allow flexibility for assigning power pins
    - Jumper wires can be used without exceeding static IR drop

<table>
<thead>
<tr>
<th>Supply Name</th>
<th>DC Resistance mOhms</th>
<th>Static IR Drop mV</th>
<th>Static IR Drop Spec mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD_O</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fixed Lead</td>
<td>15.30</td>
<td>2</td>
<td>10</td>
</tr>
<tr>
<td>Jumper Wire</td>
<td>30.72</td>
<td>4</td>
<td>10</td>
</tr>
</tbody>
</table>
Maintaining Signal Integrity
Signal Integrity

- Electrical simulation can be used to optimize via placement for improved isolation at 77GHz
  - Two alternated designs evaluated

Version 1

Version 2

- Added Vias
- Alternate Via Space
Signal Integrity

- Containment of electromagnetic fields
  - Version 2 shows improved containment of electromagnetic fields

Greatly improved Isolation
Signal Integrity

- Containment of electromagnetic fields
  - Version 2 shows improved containment of electromagnetic fields
IBIS Models
IBIS Models

- Input Output Buffer Information Specification (IBIS)
  - Method of providing the Input/Output device characteristics through V/I data
  - Tabular description of the IO buffer characteristics
  - Freescale provides IBIS models by combining Pad Driver Models with Package RLC’s into a single IBIS.
  - Package RLC’s are extracted from the completed package design using the same extraction techniques used for Power and Signal integrity inside the package.
Session Summary

• The integrated circuit package is a vital portion of overall system performance

• A well designed package will
  – Maintain power integrity
  – Insure signal integrity

• IBIS models including package parasitics enable board and system level simulation
For Further Information

- Signal Integrity [http://bethesignal.com](http://bethesignal.com)

- My Contact information
  - Neil Tracht – Manager of Package Design and Electrical Modeling
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Closing

• By now, you should be able to:
  − Describe package parasitics
  − Describe analysis techniques used to insure robust package performance
  − Describe package design considerations used to optimize package performance