System-in-Package Solutions Using Freescale’s Redistributed Chip Packaging (RCP): "How Small is the New Big"

FTF-SDS-F0249

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Introduction

• Companies are looking to differentiate.

• With Internet-of-Things (IoT), product innovation and time to market are important.

• Consumer, medical, defense and wearable products are pushing towards more integration, higher performance and smaller form-factor.

• Redistributed Chip Packaging (RCP) Technology being developed for:
  - System-in-Package (SiP).
  - μSOM (micro System-on-Module).
Agenda

• Industry direction toward more integration.

• Redistributed Chip Packaging (RCP Technology).

• Package reliability.

• SiP (System-in-Package) and µSOM (Micro System-on-Module).

• Development of the Ecosystem.

• Design and Manufacturing through Freescale.
Objective

• Show why we believe the industry will move towards more integration with smaller form-factors.

• Provide a good understanding of the Redistributed Chip Packaging (RCP) technology.
  - Show why this is more than a packaging technology.

• Understand the various levels of integration and the different components that may be considered.

• Understand areas where it may be applied and what it may mean for your specific applications.

• Show how our customers may engage with Freescale today.
1. Woman ingests personal medical device

2. Personal medical device communicates to mobile device


4. Wireless Access Network communicates to The Cloud

5. The Cloud communicates to Big Data Analysis and Application Server

6. In case of exception, communication to health care provider

7. Automated medical attention

“Analyzing trends for preventive care” (Big Data)

“Monitoring Vitals” (App Server)

“Blood pressure high”
1. Car approaching home

2. Car communicates to the Cloud

3. Cloud communicates to box in home

4. Automated anticipated home settings

- "Security in zones activated"
- "Lighting preferences"
- "Turn on oven"
- "Activate hot water heater"
- "Start downloading episodes 3"
- "Email sent: dinner time"

"now 5 km from home"

"Setting personal preferences"
SiP vs μSOM

- **SOM: System-on-Module.** Standard PWB.
- **SiP:** More than one die in a package but not necessarily a full feature module.
- **μSOM:** Same as SiP plus support components to function as a micro PWB.
  - Full feature controller.
  - Small form-factor.
  - Integrate, Plug-and-Play module.
  - Fully tested, software enables, certified (FCC, shielding, antenna, etc).

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- **Power**
  - Management
  - Generation
  - Storage
  - Scavenging

- **Memory**
  - Performance related
  - Security

- **Processor/Controller**
  - Data
  - Encryption

- **Sensing**
  - Orientation
  - Acceleration/Vibe
  - Optical/Imaging
  - Chem/Bio/Rad
  - Pressure
  - Acoustic

- **Actuating**
  - Drug delivery
  - Electrical/Mechanical Stimuli
  - Audible
  - Self destruct
  - Anti-Tampering
  - Anti-Counterfeiting

- **RF**
  - Data Telemetry
  - Communication

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Benefit of the µSOM Solution

• Provide a ‘Plug-and-Play’ module solution.

• Integrate all of the key components into a single package.
  - Integration of the hardware (Processor, Memory, PMIC, RF, voltage regulation, shielding, RLC’s, etc.).

• System routing and optimization done with the package.

• High speed interfaces done within the package.

• µSOM comes enables with firmware and software (Boot Loader, Linux OS, Android OS, other).

• Simplify board design for the customer.

• Shorten time to market for the customer.

• Provide an upgrade path for the next generation processor, memory or features.
Standard Package and SiP Approaches

Single Die Package

- Wire Bond
- Flip Chip

Multi-Chip Modules
(WB, FC, SMD)

- Agilent
- STATS ChipPAC
- Freescale

Stacked Die
(WB, FC, SMD)

- Toshiba
- ECN

Package on Package
(WB, FC, TSV, SMD)

- STATS ChipPAC
- Amkor
- ESCATEC
Additional SiP Technologies

**Double Sided Flex**
- Starkey

**Embedded Substrates**
- Imbera

**TSV/Si Interposer**
- AT&S
- Shinko
- Samsung
- AT&S
- Shinko
Freescale’s Redistributed Chip Package (RCP)

- **Why RCP: Smallest form factor with the highest level of integration!**

- FO-WLP is in high volume production today.

- High productivity, large area batch process.
  - Eliminates package substrate.
  - Eliminates wire bonds / C4 bumps.

- High performance package.
  - Reduced electrical parasitics.
  - Higher frequency response.

- Ultra Low-k Compatible (<90 nm MLM).
  - Compliant with advance Si technology.

- Pb-free, Halogen free, ROHS compliant.

- Single chip, multiple chip and embedded component capability.

- Certified to JEDEC/FSL Commercial, Industrial, Automotive Level Reliability.
RCP Development History

- RCP Technology group formation
- Created first RCP sample
- Scaled-up to 150 mm panels
- Built first electrical sample 17x17 RCP
- Purchased tools
  - Scaled up to 200mm
  - First set BOM defined
  - Mechanical RiP
- 4ML process developed
  - Electrical i.275 RiP
- 300 mm panel line defined and capital signed
  - Passed 1500 cyc TC, 144 hrs uHAST
  - Electrical 3G RiP
- 300 mm line installed
  - First 300 mm panel produced

2002
- 17 x 17 2ML
- 17 x 17 2ML

2003
- 18 x 20 4/1ML

2004
- 29 x 29 4ML

2005
- 25 x 25 4/1ML
- 30 x 30 4/1ML

2006
- 2007

2008
- 9x9 2ML (C90)
- 12x12 2ML (C65) processor NPI

2009
- 6x6 2ML PMIC certified
- 0.4 mm pitch 12x12 2ML certified

2010
- Technology transfer to HVM
- HVM line qualified

2011
- Heterogeneous 2D and 3D SiP
- Derivative Solutions
- Ultra low profile 3D
- HVM line certified

2012
- High level 3D integration
- Multi-die certified
- 77GHz radar

2013
- Imager module integration
- Fine pitch capability
- Rev2 77GHz radar

- 9x9 2ML
- 12x12 2ML
- 12x12 2ML, 0.4P
- 12x12 2ML
- 18 x 20 4/1ML
- 25 x 25 4/1ML
- 30 x 30 4/1ML
- 29 x 29 4ML
- 25 x 25 4/1ML
- 25 x 25 4/1ML
- 30 x 30 4/1ML
- 29 x 29 4ML
- 25 x 25 4/1ML
- 30 x 30 4/1ML
WLCSP vs. RCP

**WLCSP**
- Blind assembly directly on a wafer
- Pkg size = die size
- Build up process based on bumping technology
- Single RDL (Redistribution Layer)
- Exposed back side and edge of die

**RCP**
- Wafer reconstitution with probed, good die
- Space creation to accommodate more IOs and sophisticate routing
- Build up process with “Fan-out” routing
- Multiple RDLs (Redistribution Layer)
- Physical protection for die

*300 mm round panel*
- 9 x 9 mm packages
- 258 IO, 0.5 mm pitch
- 716 packages/panel
- 2 layer build-up
Freescale’s Redistributed Chip Package (RCP)

The process starts with a carrier plate
Fan-in vs. RCP Fan-out Packaging

- Fan-in Wafer level CSP
- Fan-out Single Die RCP
- Fan-out Multi Die RCP (SiP)
- Fan-out 3D RCP (SiP)
**Through Silicon Via**

- Fine geometry possible (~10µm dia)
- High aspect ratio possible (>10:1)
- Low resistance possible (<50mΩ)
- Typical uses: 2.5D, 3D-die stacking, high I/O, high bandwidth

**Through Package Via**

- Coarse geometry (~100-200µm dia)
- Lower aspect ratio (3:1 – 5:1)
- Low resistance typical (<50mΩ)
- Typical uses: 3D SiP, true heterogeneous integration

*EETimes* - P.S. Andry, et. al., IBM Journal of Research and Development

*Freescale*
Attributes

• Dramatic volumetric shrink of current and future systems.
• Increased functionality (heterogeneous integration).
• Improvement in system performance (low parasitics, low inductance).
• Weight reduction for the module.
RCP Compatible Die Design

RCP Designed  Flip Chip Die  Dual Row WB Die  Die w/ RDL

Fine Pitch Capability
Use of an RDL layer

- Tight pitch or >2 rows of bond pads.
- Escape routing harder without adding an addition RDL layer.
- Last metal layer modified at wafer level to redistribute pads toward the center of the die.
Characteristics of RCP Routing Nominal Property Values

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric thickness (nom)</td>
<td>20 um</td>
</tr>
<tr>
<td>Metal thickness (nom)</td>
<td>10 um</td>
</tr>
<tr>
<td>Buildup Dielectric constant</td>
<td>2.7-3.3 (1GHz)</td>
</tr>
<tr>
<td>Buildup Dielectric loss</td>
<td>0.02-0.03</td>
</tr>
<tr>
<td>Buildup Breakdown Voltage</td>
<td>10-15 V/µm</td>
</tr>
<tr>
<td>Panel Epoxy Dielectric Constant</td>
<td>2.5-3.5 (1MHz)</td>
</tr>
<tr>
<td>Panel Epoxy Dielectric loss</td>
<td>0.001-0.005</td>
</tr>
</tbody>
</table>
RCP Building Blocks

- Embedded SMD
- Ultra Thin Pkg Stacking with Side Connections
- High Pin Count Embedded Die
- Multiple layers of signal routing including power, ground, and signal isolation
- Embedded, RCP defined inductors
- Memory
- Thru Pkg Vias
Key Differentiators for RCP

- Volumetric Shrink 40-90%.
- Die to die spacing as close as **100µm- 250µm**.
- Package thickness ~**125µm possible**.
- Die to die connections as short as **250µm**.
- Package **inductances <50%** of wirebond solution.
- Pb-Free BGA pitch capable of **<0.4mm**
- Weight reduction for the module 20-50%.
- Wide range of heterogeneous integration.

<table>
<thead>
<tr>
<th>Integrated Elements</th>
<th>Surface mounted devices (SMD) (R,L,C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor, uController, PMIC, ASIC’s</td>
<td>Balun</td>
</tr>
<tr>
<td>RF (baseband, transceiver, ZigBee, WiFi)</td>
<td>Crystal Oscillator</td>
</tr>
<tr>
<td>GaAs, GaN IC’s</td>
<td>mmWave (Tx-PA, Rx, VCO)</td>
</tr>
<tr>
<td>FET, IGBT, RGT, SCR</td>
<td>Thin Film Resistors</td>
</tr>
<tr>
<td>FPGA’s</td>
<td>Integrated antenna</td>
</tr>
<tr>
<td>Memory (DDR, Flash, SDRAM)</td>
<td>Film Battery</td>
</tr>
<tr>
<td>MEMS (accelerometer, inertial sensor, µBolometer)</td>
<td>Ball Grid Array (BGA), Flex connectors</td>
</tr>
</tbody>
</table>
Radar Applications

for wireless product and now

Sensor Technologies for Driver Assistance Systems

<table>
<thead>
<tr>
<th>SRR</th>
<th>LRR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parking assist</td>
<td>ACC</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>ACC stop &amp; GO</td>
<td></td>
</tr>
<tr>
<td>Lane keeping support</td>
<td></td>
</tr>
<tr>
<td>Collision Warning</td>
<td></td>
</tr>
<tr>
<td>Pre-crash sensing /</td>
<td></td>
</tr>
<tr>
<td>pre-crash brake assist</td>
<td></td>
</tr>
<tr>
<td>Pre-crash collision avoidance /</td>
<td></td>
</tr>
<tr>
<td>automatic emergency brake</td>
<td></td>
</tr>
</tbody>
</table>

Comfort Functions

Safety Functions

Vehicle Guidance
NXP 77GHz Radar Chip set
4-Ch VCO, 2-Ch PA, 4-Ch Rx

Future Planning:
• Expect more levels of integration including additional functions.
RCP 3D Stacked SiP Module

- >100 components including Freescale Kinetis K60 MCU
- 3 RCP PoPoP SiP Modules mounted together.
RCP Customer Programs

Defense and Automotive

MEMS camera module

Imaging

Network night vision camera module

Sensor Array

Medical

Medical

Diagnosis capsule

Server Module
Freescale Communication µSOM’s:

**802.15.4 RCP DV**
- ZigBee

- **Certified Platform**
  - External Antenna
  - Shield
  - Disretes
  - RF Matching (Balun)
  - Crystal (25MHz)
  - RF IC (Coconino)
  - Microcontroller (K20_512)

- **µSoM**

**WiFi RCP DV**

- **Certified Platform**
  - External Antenna
  - Shield
  - Disretes
  - RF Switch/Matching
  - Crystal (25MHz)
  - RF IC¹ (QCA 4002)
  - Microcontroller² (K20_512)

- **µSoM**
MCU Connectivity: Shielding and antenna

- Enabling shielding and embedded antenna
i.MX6 Layout Options - Feasibility

**High Performance:**
- **Config:**
  - i.Mx6 DL
  - PF 100
  - SPI NOR 512Mb
  - DDR3 4Gb x 4
- **Caps:**
  - 0402 (PF100)
  - 0201 (PF100)
  - 0201 (i.MX & DRAM)

**Low Power:**
- **Config:**
  - i.Mx6 DL
  - PF 100
  - SPI NOR 512Mb
  - LPDDR2, 16Gb
- **Caps:**
  - 0402 (PF100)
  - 0201 (PF100)
  - 0201 (i.MX & DRAM)
NXP
Single Die Reliability Performance
Jedec, AEC and Customer Spec, HVM Site

- RCP 6x6mm, 105 I/O, 2ML 0.5mm pitch

<table>
<thead>
<tr>
<th>Test Item</th>
<th>Sample Size</th>
<th>JEDEC/FSL Commercial</th>
<th>JEDEC/FSL Industrial</th>
<th>AEC Grade II</th>
<th>Extended Stress</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-con: MSL3/260ºC</td>
<td>331 x 3</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>N/A</td>
</tr>
<tr>
<td>CSAM Post Pre-Con &amp; Stress</td>
<td>55 x 3</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>N/A</td>
</tr>
<tr>
<td>Temp Cycle (-55 to 125ºC) w/ MSL3/260ºC Pre-con</td>
<td>80 x 3</td>
<td>Pass 400cyc</td>
<td>Pass 700cyc</td>
<td>NA</td>
<td>Pass 1000cyc</td>
</tr>
<tr>
<td>Temp Cycle (-50 to 150ºC) w/ MSL3/260ºC Pre-con</td>
<td>80 x 3</td>
<td>NA</td>
<td>NA</td>
<td>Pass 500cyc</td>
<td>NA</td>
</tr>
<tr>
<td>THB 85ºC/85% w/ MSL3/260ºC Pre-con</td>
<td>80 x 3</td>
<td>Pass 504hrs</td>
<td>Pass 1008hrs</td>
<td>Pass 1008hrs</td>
<td>NA</td>
</tr>
<tr>
<td>uHAST 130ºC/85% w/ MSL3/260ºC Pre-con</td>
<td>80 x 3</td>
<td>Pass 96hrs</td>
<td>Pass 96hrs</td>
<td>Pass 96hrs</td>
<td>NA</td>
</tr>
<tr>
<td>HTOL 125ºC</td>
<td>80 x 3</td>
<td>Pass 504hrs</td>
<td>Pass 504hrs</td>
<td>Pass 504hrs</td>
<td>NA</td>
</tr>
</tbody>
</table>

- RCP 6x6mm, 88 I/O, 1ML 0.5mm pitch

<table>
<thead>
<tr>
<th>Test Item</th>
<th>Sample Size</th>
<th>AEC Grade II</th>
<th>AEC Grade I</th>
<th>AEC Grade 0</th>
<th>Extended Stress</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-con: MSL3/260ºC</td>
<td>80x3</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>N/A</td>
</tr>
<tr>
<td>CSAM Post Pre-Con &amp; Stress</td>
<td>11 x 3</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td>N/A</td>
</tr>
<tr>
<td>Temp Cycle (-50 to 150ºC) w/ MSL3/260ºC Pre-con</td>
<td>80</td>
<td>Pass 500cyc</td>
<td>Pass 1000cyc</td>
<td>Pass 2000cyc</td>
<td>N/A</td>
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<tr>
<td>Temp Cycle (-65 to 150ºC) w/ MSL3/260ºC Pre-con</td>
<td>80</td>
<td>NA</td>
<td>Pass 500cyc</td>
<td>N/A</td>
<td>Pass 1000cyc</td>
</tr>
<tr>
<td>uHAST 130ºC/85% w/ MSL3/260ºC Pre-con</td>
<td>80</td>
<td>Pass 96hrs</td>
<td>Pass 96hrs</td>
<td>Pass 96hrs</td>
<td>NA</td>
</tr>
</tbody>
</table>

Completed and passed AEC grade 2 certification

Certifying to AEC grade 1 and 0 along with TS16949 automotive certification

*** Mechanical Test Vehicle with CSAM and VM. Live sample test is pending test capability set up by Jan’13.
Manufacturing Strategy

High Volume Production 300mm

- Single die
  - Nepes Corp. Korea (licensee) AEC I&0 & TS16949 certification.
- 2D Multi-die
  - 2D multi-die package being certified.

Low - Medium Volume Production

- 2D Multi-die, 3D System-in-Package, Military (ITAR), Medical, US based mfg.
  - Tempe, AZ RCP line (development).
  - Chandler, AZ EPM line (manufacturing).
Engagement Models:

• **Freescale Designed Products.**
  - Design, fabrication, test, sales and support managed by Freescale.

• **Customer Specific Products.**
  - **Option A:** ASIC system including Freescale die. Total product solution may be supported through Freescale.
  - **Option B:** ASIC system design and test owned by the customer. Freescale owns package design and fabrication.
    - Managed through our Foundry services business.
RCP Prototyping – A Typical Sequence of Events

Concept Stage
1) Discussion of System/Package Construction and Requirements
2) SOW/Timeline

Quotation

Kick-off/Design Meeting
1) Schematic/Netlist/Requirements
2) Bill of Materials/Supply Chain
3) Project Management

Design and Modeling
1) Design-Cadence APD
2) Modeling-Sigrity, ABAQUS, Flowtherm

Design Review

Design Approved-Order
RCP Masks

Procurement
1) Die
2) SMDs
3) Other

RCP Fabrication
BOM to RCP Packages

RCP Shipment
1) Final Outgoing Inspection
2) Shipment

Cycle time: 1 month to ~ 4 months from concept to delivering prototypes
Designing an RCP SiP

<table>
<thead>
<tr>
<th>Item</th>
<th>Quantity</th>
<th>Value</th>
<th>Min</th>
<th>Rating</th>
<th>Tolerance</th>
<th>Dielectric</th>
<th>Already Qualified</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two die Stack: 4324 um x 3782 um (1st die, fixed) and 4000 um x 4000 um (2nd die, to-be-developed)</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Capacitor C340</td>
<td>1</td>
<td>22 uF</td>
<td>10 V</td>
<td>20%</td>
<td>X5R</td>
<td>Yes</td>
<td>C805</td>
<td></td>
</tr>
<tr>
<td>Capacitor C342, C105, C106</td>
<td>3</td>
<td>10 uF</td>
<td>16 V</td>
<td>10%</td>
<td>X5R</td>
<td>No</td>
<td>C603</td>
<td></td>
</tr>
<tr>
<td>Capacitors C309, C311, C312</td>
<td>3</td>
<td>10 uF</td>
<td>10 V</td>
<td>10%</td>
<td>X5R</td>
<td>No</td>
<td>C603</td>
<td></td>
</tr>
<tr>
<td>Capacitor C213</td>
<td>1</td>
<td>10 uF</td>
<td>16 V</td>
<td>10%</td>
<td>X5R</td>
<td>No</td>
<td>C603</td>
<td></td>
</tr>
<tr>
<td>Capacitors C325, C330</td>
<td>2</td>
<td>2.2 uF</td>
<td>10 V</td>
<td>10%</td>
<td>X5R</td>
<td>No</td>
<td>C402</td>
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<tr>
<td>Capacitors C111, C112, C113, C114</td>
<td>4</td>
<td>220 nF</td>
<td>10 V</td>
<td>10%</td>
<td>X5R</td>
<td>Yes</td>
<td>C402</td>
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</tr>
<tr>
<td>Capacitors C103, C110, C302, C303, C306, C307, C308</td>
<td>7</td>
<td>100 nF</td>
<td>16 V</td>
<td>10%</td>
<td>X5R</td>
<td>No</td>
<td>C201</td>
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<tr>
<td>Capacitors C117, C211, C212</td>
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<td>33 nF</td>
<td>16 V</td>
<td>5%</td>
<td>X5R</td>
<td>No</td>
<td>C201</td>
<td></td>
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<tr>
<td>Capacitors C203, C206</td>
<td>2</td>
<td>3.3 nF</td>
<td>16 V</td>
<td>5%</td>
<td>X5R</td>
<td>No</td>
<td>C201</td>
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</tr>
<tr>
<td>32 kHz smd Crystal 1.6 mm x 1.0 mm x 0.5 mm</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Diode protection</td>
<td>1</td>
<td>-</td>
<td>8 V</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Resistors R302, R303</td>
<td>2</td>
<td>39 k</td>
<td>0.125W</td>
<td>1%</td>
<td>-</td>
<td>C201</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resistor R301</td>
<td>1</td>
<td>1 k</td>
<td>0.125W</td>
<td>1%</td>
<td>-</td>
<td>C201</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bill of Materials

System Schematic/BDIF
SiP RCP Design Rules

- Design rules for RCP SiP released.
- Captures typical SiP elements including vias, SMD capture pads, SMD/die/EGP/TPV dimensional rules.
Designing an RCP SiP

Sample Build

RCP SiP Design

Simulation

Evaluation
Summary

• RCP System-in-Package has been developed as a universal platform for:
  - Heterogeneous integration.
  - System miniaturization.
  - System performance.

• The technology is maturing rapidly with IC partners and customers working closely with Freescale to develop the infrastructure to support volume production.
  - Single die prototyping and production available today.
  - SiP and µSOM prototyping available today and plans underway to support volume production.

• Structure in place to support ITAR, US based development and volume manufacturing.

• Structure in place to support high volume production through our subcon partner Nepes.
RCP Contacts

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