Power Conversion Using Freescale Digital Signal Controllers and Kinetis V Series Microcontrollers

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Objective: Review challenges of digital power control systems and show how digital signal controllers are helping to meet the growing requirements.

Agenda:
- Digital Power Trends and Landscape
- Digital Signal Controller Product Overview
- Kinetis V Series MCUs Overview
- Key Peripherals for Digital Power
- Resonate Converter Introduction
- Application Example: Digital Control of LLC Resonant Converter
- Q&A
Next Generation Energy Landscape

- Mobile Power Adapter
- Low End Wireless Charger
- Ceiling Fans
- Hand Held Tools
- Power Factor Correction
- Offline Solar Inverter
- Single Motor Control
- Micro Inverter
- Wireless Charger
- Battery Inverter
- Digital Power – 1-phase
- Sensorless Motor Control
- Server Power Supply
- Micro Inverter
- Induction Hob – 2 burners
- Dual Motor Control
- Industrial Motor Control
- Induction Hob – 4 burners
- Digital Power - 3ph
- Multilevel Inverter
- Online UPS
- Grid Tied Solar Inverter

Application Complexity

- 25-35 MHz core
  - High Res PWM
  - Low power consumption
  - 12-bit ADC @ 1uS
  - Small memory
  - Very cost sensitive

- 35-50 MHz core
  - High Res PWM
  - Reduced power consumption
  - 12-bit ADC @ 1uS to 500nS
  - Mid size memory
  - Cost sensitive

- 60 MHz core
  - High Res PWM
  - System integration

- 80 MHz core
  - 12-bit ADC @ <500nS
  - System integration
  - Improved math features

- 100 MHz core
  - Very High Res PWM
  - 12-bit ADC @ <500nS
  - Flash >128kB
  - System integration
  - Improved math features
Where Is Digital Power Conversion Applied?

“Digital power Conversion” is a power system that is controlled by digital circuits, in much the same way as would be with analog circuits, to monitor, supervise, communicate and control looping. A fully digitally controlled power system includes both digital control and digital power management.

**Digital Control**
- The control feedback or feed-forward loop, which is controlled by the digital circuit or programmable controller, regulates the output of the power system by driving the power switch duty cycle using pulse width modulation techniques.
- The control circuits combine A/D conversion, Pulse Width Modulation, and Communication interfaces, operating entirely or mostly in digital mode.

**Digital Power Management**
- A Digital circuit or programmable controller provides the functions of configuration, tracking, monitoring, protection, supply sequencing, and communication with the environment.
Comparison of Analog and Digital Power Control System

Analog Control System With Digital Management

Full Digital Control System

Both MCU and Analog PWM controller is replaced by one DSC
Analog Control vs. Digital Control
- Transient Response Comparison

**Traditional Analog control**
- Constant Voltage
- Constant Power
- Power Fold Down
- Advanced Digital control

**Constant Current**

**Basic Analog control**
- Constant Voltage
- Constant Power
- Constant Current

**Advanced Digital control**
- No OV and no OC during transient because of the smooth loop transition
- Output profile is programmable

**Constant Voltage**

Over voltage during load step-down

Over current during load step-up

**Iout**

**Vout**

**Iout**
Digital vs. Analog Control Loop

Benefit of digital control:
1. 1) Optimize feedback loop to meet application requirements
2. 2) Runtime changes to compensation parameters according to operating conditions
The differences between hard switch and soft switching

<table>
<thead>
<tr>
<th>Hard Switching</th>
<th>Soft Switching</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast transition rate during on-off transition</td>
<td>Moderate transition rate during on-off transition</td>
</tr>
<tr>
<td>Overlaps between transitions of voltage and current</td>
<td>Either zero voltage switching or zero current switching</td>
</tr>
<tr>
<td>High noise generation and switch loss</td>
<td>Low noise generation and very low switch loss</td>
</tr>
</tbody>
</table>

Benefits of soft switching

- Greatly reduce over-all electro-magnetic emissions over a wide frequency spectrum
- Higher system efficiency and less heat dissipation will result in increasing the power density of the system
Transfer Function Of Control Loop

- $V^*_o$ is the reference; $V_o$ is the output; $K_{vs}$ is the feedback gain.
- Control loop includes a PID controller and a power stage model.
- PID controller is a dynamic error regulator

![Diagram showing PID transfer function and Power Stage transfer function]
Control Law Processor - PID Controller
(Proportional-Integral-Derivative)

- **Continuous (Analog) Expression**

  \[ M(t) = K_p e(t) + K_i \int e(t) dt + K_d \frac{d}{dt} e(t) \]  

  \[ e(t) = X_i(t) - X_f(t) \] 

  \[ m(n) = K_p e(n) + K_i \sum_{i=0}^{n} e(i) \Delta t + K_d \frac{e(n) - e(n-1)}{\Delta t} \] 

  \[ m(n) = m(n-1) + K_p [e(n) - e(n-1)] + K_i e(n) \Delta t + K_d \frac{e(n) - e(n-1)}{\Delta t} - \frac{e(n-1) - e(n-2)}{\Delta t} \]

  Where -- \( e(t) \): Error signal; \( K_p \): Proportional Gain; \( K_i \): Integral Gain; \( K_d \): Derivative Gain
Conversion To Z-Transformation

\[ z[e(n-1)] = z^{-1}E(z) \quad \& \quad z[ \sum_{i=1}^{n} e(n)] = \frac{E(z)}{1 - z^{-1}} \]

From Equation (4)

\[ G_{VEA}(z) = \frac{M(z)}{E(z)} = K_{pv}^* + \frac{K_{iv}^*}{1 - z^{-1}} + K_{id}^* (1 - z^{-1}) \quad -(5) \]

Where: \( K_{pv}^* = K_p ; \quad K_{iv}^* = K_i \times \Delta t ; \quad K_{id} = K_d \div \Delta t \)

Digital PID Controller

\[ E(z) \quad \rightarrow \quad K_{pv}^* \quad \rightarrow \quad K_{iv}^* \left(1 - z^{-1}\right) \quad \rightarrow \quad + \quad M(z) \]

\[ e(n) \quad \rightarrow \quad \rightarrow \quad K_{id}^* \left(1 - z^{-1}\right) \quad \rightarrow \quad + \quad m(n) \]
Power stage Z-transformation function

\[ G_v(S) = \frac{\tilde{V}_o}{\tilde{V}_{vo}} = \frac{K}{SCV_o} \]

\( \tilde{V}_o \) and \( \tilde{V}_{vo} \) are values of output and loop output

\[ G_{vh}(z) = Z(G_{vh}(S)) = (1 - z^{-1})Z[\frac{G_v(S)}{S}] = \frac{K \cdot T_s}{CV_o(z - 1)} \]
Measurement criteria for a stable closed loop system
- Phase margin should be greater than 45° at open loop cross frequency

\[ \angle G_{v\text{--}open}(e^{j\omega_c T_s}) > -180° + 45° \text{ at where } \left| G_{v\text{--}open}(e^{j\omega_c T_s}) \right| = 1 \]

- Gain margin should be greater than one at the frequency where the phase shift is -180°

\[ \frac{1}{\left| G_{v\text{--}open}(e^{j\omega_c T_s}) \right|} > 1 \text{ at where } \angle G_{v\text{--}open}(e^{j\omega_c T_s}) = -180° \]
## Compare Digital Control To Analog Control

<table>
<thead>
<tr>
<th></th>
<th>Analog Control</th>
<th>Digital Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control Circuit</td>
<td>Complex, Bulky</td>
<td>Simple, Programmable, Integrated</td>
</tr>
<tr>
<td>Flexibility</td>
<td>Bad</td>
<td>Good</td>
</tr>
<tr>
<td>Design Continuity</td>
<td>Bad</td>
<td>Good</td>
</tr>
<tr>
<td>Sample Mode</td>
<td>Continuous</td>
<td>Digitalization Error</td>
</tr>
<tr>
<td>Processing</td>
<td>Continuous</td>
<td>Control Delay</td>
</tr>
</tbody>
</table>
Digital Controlled Power Supply

EMI Filter → PFC → Option: High Voltage Buck or Boost → Synch Rectifier → Output Filter

Switching Regulator → MOSFET → PWM Isolator → PWM Regulator

Primary side Digital Controller: Vdd, ADCs, PWMs

Secondary side Digital Controller: PWMs, Vdd, ADCs, GPIOs

Back Panel Connector
Benefits of Digital Power

- **Free from** the effects of **component tolerance**, parametric drift, aging, etc.
- **Configurable** feedback loop **structure** for specific application requirements
- **Adaptive control** to meet changing operating conditions
- **Flexible** Pulse Width **Waveform-generation** module
- **Programmable relationships** among **PWM** outputs
- **Upgradeable** with new features **without hardware** changes
- **Retainable** operational **data** for diagnostic and record keeping
- **Diverse communications** capabilities
- **Reduced** component count and **cost**
- **Higher** power density due to overall **integration**
- **Shorter R&D cycle**, fewer turns of board prototyping
- **Portable Projects** for faster reuse
- **Defendable firmware**—protects IP and differentiating technology
Freescale Power Conversion Solutions

FSL Solutions

- 8/16/32 bit MCU and DSC
- Power MPU
- i.MX MPU
- RF/Wireless
Digital Signal Controller Product Overview
• Ease of use of a microcontroller (MCU) and the processing power of a digital signal processor (DSP)

• Reduced complexity and latency with simplified memory structure, shadowed register set, interrupt prioritization and cache

• 32-bit core improves precision without compromising performance

• Portfolio scales to exactly fit the applications needs

• Flexible cores scale from 32MHz to 100MHz

• Flash extends from 12kB to 256kB with additional Flex Memory

• Packages range from 28pins to 100pins

• Very high speed ADCs capture events real time

• High resolution PWMs improve switching efficiency and control performance

• Flexibility with the crossbar to simplify pin out and peripheral inter-connection

• DMA to reduce CPU overhead

• Enhanced customer experience via integrated tools and reference designs

• Code reusable across the complete portfolio

• Extensive S/W libraries provide quick project ramp up

Winning with Freescale DSC in Digital Power Conversion & Motor Control
What is Digital Signal Controller?

• Specialized microprocessor whose architecture contains a core engine capable of competitively performing both microcontroller and digital signal processor functionalities

• Core processing capability applicable to many types of system solution

• Common basic features:
  - MAC, single instruction cycle allowing several memory accesses, address generation units, algorithms for efficient looping

• Specialized cost effective, high performance on-board interfaces utilized in implementing embedded control applications:
  - PWM; multifunction timer; high speed ADCs; DACs; Comparators; SCIs (UART); SPIs; CANs and I2Cs, etc.

• Embedded nonvolatile memory:
  - Flash memory, ROM or EEPROM

• Easy to use development tools
56800/E Family Combining Signal Processing and Controller Functionality

Traditional Microcontroller

- Designed for Controller Code
- Compact Code Size
- Easy to Program
- Inefficient Signal Processing

Traditional DSP Engine

- Designed for DSP Processing
- Designed for Matrix Operations
- Complex Programming
- Less Suitable for Control

- Instructions Optimized for Controller Code, DSP, Matrix Operations
- Compact Assembly and “C” Compiled Code Size
- Easy to Program
- Additional MIPS Headroom and extended addressing space
DSP56800E Core Features

<table>
<thead>
<tr>
<th>CPU</th>
<th>MIPS</th>
<th># Interrupt Priorities</th>
<th>Registers</th>
<th>Data Types</th>
<th>Program Memory Adr Space</th>
<th>Data Memory Adr Space</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP56800E</td>
<td>120 from RAM 60 from Flash</td>
<td>5</td>
<td>7 Data 8 Address</td>
<td>8-bit, 16-bit 32-bit</td>
<td>4 MB</td>
<td>32 MB</td>
<td>Fully Synthesizable and Scanable</td>
</tr>
</tbody>
</table>

### 56800/E MCU Functionality
- True Software Stack and Pointer
- 16-bit Program Word
- 20 Addressing Modes and Atomic Read-Modify-Write Instructions
- General Purpose Register Files and Orthogonal Instructions to Data and Address Register Files
- Full Set of Bit and Bitfield Manipulation Instructions and 16- and 32-bit Shifting
- Superfast Interrupt

### 56800/E DSP Functionality
- Multiplier - Accumulator (MAC) Single And Dual Parallel Move Instructions
- No Overhead Hardware Looping Nested Looping Capability
- Modulo arithmetic (For Circular Buffers) Integer and Fractional Arithmetic Support
- Nested Interrupt with HW priority Fast Interrupt Support
Mapping the Architecture to DSP Algorithms

**Common Operation in DSP**
- MAC X0, Y0, A
- X:(R4)+, Y1
- X:(R3)+, C

**Arithmetic Op**
- 1st Read
- 2nd Read

**Operations Performed:**
- Multiply-Accumulate
- 3 Memory Accesses
- 2 Address Additions

**Instruction Fetch:**
- PAB - 21 bits
- PDB - 16 bits

**1st Data Access:**
- XAB1 - 24 bits
- CDBR - 32 bits

**2nd Data Access:**
- XAB2 - 24 bits
- XDB2 - 16 bits

**Common Operation in DSP**

**Program Memory**

**Data Memory**

**IP-Bus Interface**

**External Bus Interface**

**Mapping the Architecture to DSP Algorithms**

**Common Operation**

**MAC X0, Y0, A**
- X:(R4)+, Y1
- X:(R3)+, C

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- CDBR - 32 bits

**2nd Data Access:**
- XAB2 - 24 bits
- XDB2 - 16 bits
MC56F84xxx Core Improvements

New instructions, providing full 32-bit compatibility

• 32 x 32 -> 32/64 Multiply and MAC Instructions
  – MAC32 - Integer Multiply-Accumulate 32 bits x 32 bits -> 32 bits
  – IMPY32 - Integer Multiply 32 bits x 32 bits -> 32 bits
  – IMPY64 - Integer Multiply 32 bits x 32 bits -> 64 bits
  – IMPY64UU - Unsigned Integer Multiply 32 bits x 32 bits -> 64 bits
  – MAC32 - Fractional Multiply-Accumulate 32 bits x 32 bits -> 32 bits
  – MPY32 - Fractional Multiply 32 bits x 32 bits -> 32 bits
  – MPY64 - Fractional Multiply 32 bits x 32 bits -> 64 bits
  – Multi-Bit Clear-Set instruction to improve flexibility of peripheral register handling

Other features

• Bit reversed address mode for FFT algorithms
• Swap all address generation unit registers with shadowed registers to reduce interrupt context switch latency
Control Law Processor - PID Controller
(Proportional-Integral-Derivative)

- **Continuous (Analog) Expression**

  \[ M(t) = K_p e(t) + K_i \int_0^t e(t) \, dt + K_d \frac{d}{dt} e(t) \]  

  Where \( e(t) = X_i(t) - X_f(t) \)

- **Difference (digital) Expression**

  \[ m(n) = K_p e(n) + K_i \sum_{i=0}^{n} e(i) \Delta t + K_d \frac{e(n) - e(n-1)}{\Delta t} \]  

  \[ m(n) = m(n-1) + K_p [e(n) - e(n-1)] + K_i e(n) \Delta t + K_d \left[ \frac{e(n) - e(n-1)}{\Delta t} - \frac{e(n-1) - e(n-2)}{\Delta t} \right] \]
Digital Control Algorithms
Accessing Coefficients & Samples

- Any Control Algorithm being converted to digital world is the digital filter
- Digital Signal Controller is Specialized microprocessor whose architecture contains a core engine capable of competitively performing both microcontroller and digital signal processor functionalities

FIR equation: \[ Y(n) = \sum_{i=0}^{N-1} C(i) \times X(n-i) \]

A/D Samples:

X memory

\[
\begin{array}{c}
X(n) \\
X(n-1) \\
X(n-2) \\
X(n-3) \\
X(n-4) \\
X(n-5) \\
X(n-6) \\
X(n-7) \\
\end{array}
\]

X memory

\[
\begin{array}{c}
C(0) \\
C(1) \\
C(2) \\
C(3) \\
C(4) \\
C(5) \\
C(6) \\
C(7) \\
\end{array}
\]
Freescale DSC Roadmap

- **MC56F800x**
  - MC56F800x – 32MHz
  - Hi Res PWM, ADC

- **MC56F802x/3x**
  - MC56F802x – 32MHz
  - Hi Res PWM, CAN, ADC, DAC, ACMP
  - MC56F803x – 32MHz
  - Hi Res PWM, CAN, ADC, DAC, ACMP

- **MC56F801x**
  - MC56F801x – 32MHz
  - Hi Res PWM, ADC

- **MC56F824x/5x**
  - MC56F824x – 60MHz
  - 64K Flash
  - Ultra-Hi Res PWM, UHS ADC, XBar
  - MC56F825x – 60MHz
  - 256K Flash
  - Ultra-Hi Res PWM, UHS ADC, XBar

- **MC56F82xxx**
  - MC56F824xx/5x
  - MC56F825x – 60MHz
  - 256K Flash
  - Ultra-Hi Res PWM, UHS ADC, XBar
  - MC56F847xx – 100MHz
  - 256K Flash
  - DMA, UHS ADC, Ultra-Hi Res PWM, XBar, DAC, ACMP, CAN

- **MC56F83xx**
  - MC56F83xx – 60MHz
  - 48 - 256K Flash
  - Large capacity

- **MC56F844xx**
  - MC56F844xx – 60MHz
  - 256K Flash
  - Ultra-Hi Res PWM, XBar, DAC, ACMP, CAN

- **MC56F85xxx**
  - MC56F85xxx – 80MHz
  - 32-bit Core
  - 512K Flash
  - DMA, UHS ADC, Ultra-Hi Res PWM, XBar, DAC, ACMP, CAN

- **MC56F80xxx**
  - MC56F801x – 32MHz
  - Hi Res PWM
  - ADC

- **New**
  - MC56F801xx
  - MC56F801xx – 32MHz
  - Hi Res PWM, ADC

- **New**
  - MC56F80xx
  - MC56F80xx – 32MHz
  - Hi Res PWM, ADC

- **New**
  - MC56F83xx
  - MC56F83xx – 60MHz
  - 48 - 256K Flash
  - Large capacity

- **New**
  - MC56F84xxx
  - MC56F84xxx – 60MHz
  - 256K Flash
  - Ultra-Hi Res PWM, XBar, DAC, ACMP, CAN

- **New**
  - MC56F85xxx
  - MC56F85xxx – 80MHz
  - 32-bit Core
  - 512K Flash
  - DMA, UHS ADC, Ultra-Hi Res PWM, XBar, DAC, ACMP, CAN

- **New**
  - MC56F800x
  - MC56F800x – 32MHz
  - Hi Res PWM, ADC
New Freescale DSC Products

Microcontrollers Based on 32-bit Hawk 56800EX core in Freescale’s 90nm TFS

- Starting below $1.00
- Cost & Performance optimized for ....
  - Advanced control loop algorithm development
  - And critical high speed timing applications
- Including
  - Advanced Motor Control (Sensorless VOC)
  - Solar Inverters
  - Server & Telecom Power Supplies
  - UPS
  - Power Adapters
  - Board Level Power Supplies
  - Low Cost Power Line Modem
  - And much more...........

- 50MHz Flash / 100MHz SRAM
- 60MHz
- 80MHz - Digital Power
- 100MHz - Digital Power
- 80MHz - Dual Motor Control

QFN

LQFP

32pin 44 pin 48pin 64pin 80pin 100pin
### Key Features:

#### Core
- **56800EX Hawk V3 @ 100MHz**
  - Supporting fractional arithmetic with 4 ACC, a pipeline depth of 8 cycles, separate program and data memory maps, nested looping, and a superfast interrupt far outpacing any competitive core on the market.

#### System
- **Intermodule Cross-Bar** directly connecting any input and/or output with flexibility for additional logic functions (AND/OR/XOR/NOR)
- **DMA controller** for reduced core intervention when shifting data from peripherals
- **Memory resource protection unit** to ease safety certification

#### Timers
- **eFlexPWM** – Freescale’s most advance timer for Digital Power Conversion with up to 8ch and 312pico-sec resolution, supported by 4 independent time bases, with half cycle reloads for increased flexibility and best in class performance
- **NanoEdge placer** to implement fractional delays

#### Analog
- **2x12-bit high-speed ADCs** each with 330ns conversion rates
- **16 ch 16b SAR ADC** that enables external sensors inputs and accurate system measurements
- **4 analog comparators** with integrated 6-bit DACs that can enable emergency shutdown of the PWMs
- **Integrated PGAs** to increase the accuracy of ADC conversions on small voltages and currents

#### Others
- 5-volt tolerant I/O for cost-effective board design
- Freescale FlexMemory for simplified data storage

#### Packages
- 48LQFP, 64LQFP, 80LQFP, 100LQFP

### Diagram

<table>
<thead>
<tr>
<th>Core</th>
<th>System</th>
<th>Memories</th>
</tr>
</thead>
<tbody>
<tr>
<td>56800EX Hawk V3</td>
<td>Memory Resource Protection</td>
<td>Program Flash up to 256KB</td>
</tr>
<tr>
<td>100MHz</td>
<td>Address Generation Unit (AGU)</td>
<td>SRAM up to 32KB</td>
</tr>
<tr>
<td></td>
<td>Data Arithmetic Logic Unit</td>
<td>FlexMemory 32KB Flash or 2KB</td>
</tr>
<tr>
<td></td>
<td>Enhanced On-Chip Emulation</td>
<td>EEPROM</td>
</tr>
<tr>
<td></td>
<td>EOnCE</td>
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</tbody>
</table>

### Timers

- **eFlexPWM**
- **NanoEdge Placer**
- **16-bit Timer**

### Analog

- **8ch HS 12-bit ADC w/PGA**
- **12bit DAC**
- **4 x Analog CMP with 6bit DAC**
- **16ch 16-bit SAR ADC**

### Communication Interfaces

- **2x I²C/SMBus**
- **3xUARTs**
- **3xSPI**
- **FlexCAN**

### Clocks

- **Phase Lock Loop**
- **Crystal OSC**
- **8MHz OSC**
- **32kHz OSC**

---

**IN PRODUCTION**
MC6F827xx

Key Features:

Core
- 56800EX Hawk V3 @ 50/100MHz supporting fractional arithmetic with 4 ACC, a pipeline depth of 8 cycles, separate program and data memory maps, nested looping, and a superfast interrupt far outpacing any competitive core on the market.

System
- Intermodule Cross-Bar directly connecting any input and/or output with flexibility for additional logic functions (AND/OR/XOR/NOR)
- DMA controller for reduced core intervention when shifting data from peripherals
- Memory resource protection unit to ease safety certification

Timers
- eFlexPWM – Freescale’s most advance timer for Digital Power Conversion with up to 8ch and 312pico-sec resolution, supported by 4 independent time bases, with half cycle reloads for increased flexibility and best in class performance
- NanoEdge placer to implement fractional delays

Analog
- 2x12-bit high-speed ADCs each with 800ns conversion rates
- 4 analog comparators with integrated 6-bit DACs that can enable emergency shutdown of the PWMs
- Integrated PGAs to increase the accuracy of ADC conversions on small voltages and currents

Power Consumption:
- Less than 0.4mA/Mhz at full speed run

Others
- 5-volt tolerant I/O for cost-effective board design

Packages
32QFN (5x5), 32LQFP, 48LQFP, 64LQFP
Key Features:

**Core**
- 56800EX Hawk V3 @ 50MHz supporting fractional arithmetic with 4 ACC, a pipeline depth of 8 cycles, separate program and data memory maps, nested looping, and a superfast interrupt far outpacing any competitive core on the market.

**System**
- Intermodule Cross-Bar directly connecting any input and/or output with flexibility for additional logic functions (AND/OR/XOR/NOR)
- DMA controller for reduced core intervention when shifting data from peripherals
- Memory resource protection unit to ease safety certification

**Timers**
- eFlexPWM – Freescale’s most advance timer for Digital Power Conversion with up to 8ch and 312pico-sec resolution, supported by 4 independent time bases, with half cycle reloads for increased flexibility and best in class performance
- NanoEdge placer to implement fractional delays

**Analog**
- 2x12-bit high-speed ADCs each with 800ns conversion rates
- 4 analog comparators with integrated 6-bit DACs that can enable emergency shutdown of the PWMs
- Integrated PGAs to increase the accuracy of ADC conversions on small voltages and currents

**Power Consumption:**
- Less than 0.5mA/Mhz at full speed run

**Others**
- 5-volt tolerant I/O for cost-effective board design

**Packages**
- 32QFN (5x5), 32LQFP, 48LQFP
Kinetis V Series MCU Overview
Kinetis V Series MCUs
Motor & Power Control

• Full Kinetis MCU portfolio compatibility targeting low cost, stand-alone motor control, to high-performance digital power conversion

• Optimized for processing efficiency with performance ranging from 75 MHz to beyond 240 MHz

• ARM architecture with best-in-class, high speed capture and control peripherals for motor control and power management applications

• Enablement and tools built around reducing customer development time and cost, whilst increasing ease of use.
## Kinetis V Series

<table>
<thead>
<tr>
<th>Device Family</th>
<th>Core &amp; Performance</th>
<th>Positioning</th>
</tr>
</thead>
<tbody>
<tr>
<td>KV1x</td>
<td>M0+ @ 75MHz</td>
<td>Low cost, entry level, 3 phase FOC BLDC solution,</td>
</tr>
<tr>
<td>KV2x</td>
<td>M0+ @ 75MHz M56800EX @ 100MHz</td>
<td>Black box solution for Motor Control</td>
</tr>
<tr>
<td>KV3x</td>
<td>M4 @ 100 &amp;120MHz</td>
<td>Mid Range solution building on Kinetis K family, Wide memory range, Floating Point</td>
</tr>
<tr>
<td>KV4x</td>
<td>M4 @ 150MHz</td>
<td>High Performance, small memories, integrates DSC ADC &amp; PWM IP for best in class performance.</td>
</tr>
<tr>
<td>KV5x</td>
<td>M4 @ 200MHz</td>
<td>Large memory blocks, integrates DSC ADC &amp; PWM IP for best in class performance.</td>
</tr>
<tr>
<td>KV6x</td>
<td>M4 @ 200MHz M4 @ 100MHz</td>
<td>Dual core solution for multi-domain environment; M4 controlling Motor, M4 for communications, controlling house keeping &amp; safety tasks</td>
</tr>
<tr>
<td>KV7x</td>
<td>M Series @ 240MHz</td>
<td>Next generation ARM Cortex Solution. Limited internal memory with excellent communications to external memories.</td>
</tr>
</tbody>
</table>
**Kinetis V Series MCUs: Scalable Solution**

**Increasing performance and integration**

<table>
<thead>
<tr>
<th>Core</th>
<th>Memory</th>
<th>Motor Control Timers</th>
<th>Enhanced Timers</th>
<th>ADC</th>
<th>LQFP PinOut</th>
<th>CMP</th>
<th>DAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>MKV4x 150MHz</td>
<td>256kB Flash</td>
<td>2 x 8Ch FlexTimer</td>
<td>12Ch eFlexPWM w/Nano Edge</td>
<td>2 x 240nS</td>
<td>100 &amp; 64</td>
<td>4x CMP with 6b DAC</td>
<td>1 x 12b DAC</td>
</tr>
<tr>
<td>MKV3x 100/120MHz</td>
<td>128-512kB Flash</td>
<td>2 x 8Ch FlexTimer</td>
<td>None</td>
<td>2 x &lt; 1uS</td>
<td>100, 64, 48 &amp; 32</td>
<td>2x CMP with 6b DAC</td>
<td>1 x 12b DAC</td>
</tr>
<tr>
<td>MKV1x 75MHz</td>
<td>32kB Flash</td>
<td>1 x 6Ch FlexTimer</td>
<td>None</td>
<td>2 x &lt; 1uS</td>
<td>48 &amp; 32</td>
<td>2x CMP with 6b DAC</td>
<td>1 x 12b DAC</td>
</tr>
</tbody>
</table>

**Scalable IP according to application needs**
Kinetics V Series KV1x – Key Messages

From the market leader in motor control MCUs -
A high performance, cost-optimized and best-in-class enabled 32-bit ARM Cortex-M0+ MCU for low/mid range Brushless DC and PMSM Motor Control applications

**Leadership**

- **Reputation & heritage** – >20 years of motor control processor development spanning multiple MCU & DSC architectures. Now includes next-generation 32-bit ARM Cortex MCUs
- **Systems Expertise** – Motor Control Centre of Excellence with >170 yrs of combined expertise in product development and OEM customer support. Extensive library of reference designs and software libraries covering all motor technologies
- **Kinetics V Series** – 6th Kinetics MCU family with KV1x as the entry point. Additional hardware & software compatible V Series families throughout 2014 with scalable performance, memory and feature integration

**Performance**

- Highest performance 75MHz clocked ARM Cortex M0+ MCU with hardware divide & square root blocks - **combined 35% performance advantage** vs. comparable ARM Cortex-M0 MCUs provides cost-reduction path for BLDC/PMSM designs.
- **2x 16-bit ADCs with 835nS conversion** time – fast current and voltage phase measurement with reduced input jitter and improved control loop accuracy
- **Flexible Motor Control Timers** – fast, high accuracy PWM generation with integrated power factor correction or speed/position sensor measurement. 12-bit DAC & Analog Comparators reduce BOM cost and provide fast, accurate over-current/voltage protection with PWM safe state shutdown

**Enablement**

- Freescale Tower MCU & Motor Driver modules, CodeWarrior IDE with Processor Expert and Cortex-M0+ math/motor control libraries. ARM ecosystem support
- Freemaker – free, run-time debugging and data visualization tool. Continual motor operation during debug. Free MCAT (Motor Control Application Tuner) plug-in simplifies the set-up and tuning of motor control algorithms
- Motor Control Toolbox – plug-in for MATLAB™/Simulink™ environments that generates initialization routines, device drivers, and includes a real-time scheduler for motor control algorithms
# Kinetis V Series KV1x MCU: Features and Benefits

<table>
<thead>
<tr>
<th>Features</th>
<th>Benefits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cortex M0+ @75MHz</td>
<td>Fastest Cortex M0+ in the market enables PMSM motor control with a M0+ solution</td>
</tr>
<tr>
<td>Hardware Square Root &amp; Divide Hardblock</td>
<td>26% performance improvement running math intensive applications such as Sensorless FOC algorithms</td>
</tr>
<tr>
<td>Dual ADC Blocks @ 835nSec conversion time</td>
<td>Capture current &amp; voltage simultaneously for the most accurate result</td>
</tr>
<tr>
<td>4ch DMA</td>
<td>Further improvements in performance realized through increased CPU bandwidth-</td>
</tr>
<tr>
<td>6ch FlexTimer + 2x2ch FlexTimer</td>
<td>Motor control PWM generation with integrated PFC, or integrated speed sensor decoder (incremental decoder / hall sensor)</td>
</tr>
<tr>
<td>Integrated 6b DAC &amp; CMP</td>
<td>Reduce BOM costs with integrated components for over current over voltage fault detection</td>
</tr>
<tr>
<td>Peripheral Interconnection</td>
<td>ADC and CMP interconnected with PWM and PDB for real time hardware control.</td>
</tr>
<tr>
<td>Light weight peripheral and memory configuration</td>
<td>Enough performance for the majority of Motor Control applications, with the right amount of memory to fit complex motor control algorithms</td>
</tr>
<tr>
<td>Dual Watchdog</td>
<td>IEC60730 Compliant solution</td>
</tr>
</tbody>
</table>
Key Peripherals For Digital Power
Memory Capability

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- On-chip memory
  - Up to 256 KB program/data flash memory
  - Up to 32 KB dual port data/program RAM
  - Up to 32 KB FlexNVM, which can be used as additional program or data flash memory
  - Up to 2 KB FlexRAM, which can be configured as enhanced EEPROM (used in conjunction with FlexNVM) or used as additional RAM
What FlexMemory is?

User Configurable As...

EEPROM:
- Eliminates external component
  - Lower system cost
- No system resources required
  - Easier implementation over emulation
- High endurance
  - Up to 10 million cycles
- High performance
  - Fast write time = ~100 uSec
  - Erase+write = 1.5mSec

Additional Data Flash:
- Flexibility
  - Space for future expansion needs
- Efficient
  - Read-while-write with the main program Flash
- High endurance data memory

Or Combination of Both
The eFlexPWM architecture is configurable, up to 4 sub-modules (shown).
eFlexPWM Sub-Module Detail

Clock → Prescaler → 16 bit counter → 16 bit comparator

Aux Clock (sub-module 0 only)

Compare 0 value

Preload

Compare 1 value

Mid-cycle reload

Reload Logic

Module counter value

Master Reload (sub-module 0 only)

Master Sync (sub-module 0 only)

Counter preload mux

Compare 2 value

16 bit comparator

Init Value

Initialize

PWM on

Comp. vs Indep.

Dead Time Generator

PWM Select Logic

Fault inputs from module bus

PWM on

Output Triggers

Interrupts

Register reload mux

Compare 3 value

16 bit comparator

Init Value

Initialize

PWM off

PWMX

Pin Mux

PWM23

Comp. vs Indep.

Dead Time Generator

PWM Select Logic

Fault protection

PWM45

Output override control

PWMMA

PWMWB

Register reloads
Center-aligned PWM Example

When the Init value is the signed negative of the Modulus value, the PWM module works in signed mode. Center-aligned operation is achieved when the turn-on and turn-off values are the same number, but just different signs.
Edge-aligned PWM Example

- VAL1 ($0100)
- VAL5 ($0000)
- VAL3
- INIT ($FF00)
- VAL2, VAL4 = $FF00

All PWM-on values are set to the init value, and never changed again. Positive PWM-off values generate pulse widths above 50% duty cycle. Negative PWM-off values generate pulse widths below 50% duty cycle. This works well for bipolar waveform generation.
In this example, both PWMs have the same duty-cycle. However, the edges are shifted relative to each other by simply biasing the compare values of one waveform relative to the other. Alternatively, if the waveforms are generated by different sub-modules, the waveforms can be shifted by simply changing the Init value of one sub-module relative to the other.
Dead Time Insertion

PWMAx

0

1

DBLPWM

DBLEN

PWMBx

0

1

IPOL

DTCNT0

start

down counter

PWMAx

0

1

PWMBx

INDEPENDENT

down counter

DTCNT1

start

rising edge detect

falling edge detect
Challenge of Controlling Resonate Converter

Challenge:
- Wide range of PWM switching frequency from 100KHz up to 1Mhz
- Need to make a change to the PWM period without changing the duty cycle for up to 4 channels of PWM within one period of the existing PWM
- PWM period change must be in a few nanosecond

Solution:
- High speed digital PWM plus Analog edge delay
- PWM duty cycles are calculated by high speed controller
- Special circuit is used to automatically increment the PWM period by repositioning edges

![Diagram showing PWM periods and edges](attachment://diagram.png)
eFlexPWM Detail Showing Inclusion of Fractional Delays
Digital adder for frequency control

- Need to calculate the next edge position for rising and falling edges within very short period.

- Software not fast enough so need hardware adder.

- Diagram shows 21 bit adder to control both edges automatically setting new comparator values after each edge has been triggered.
ADC Channel Scan Modes

Once
- The ADC starts to sample just one time whether you use the START bit or by a sync pulse. This mode must be re-armed by writing to the ADCR1 register again if you want to go capture another scan.

Triggered
- Sampling begins with every recognized START command or sync pulse.

Loop
- The ADC continuously take samples as long as power is on and the STOP bit has not been set.

Sequential Mode
- Sequential will sample SampleN one after another. Channel ANAx are sampled by ADCA and Channel ANBx are sampled by ADCB.

Parallel Mode
- Simultaneous: Parallel can sample SampleN from Group1 and SampleN from Group 2 at the same time.
- Independent: ADCA and ADCB can operate independently. At end of scan of each ADC, they generate separate interrupt request.
A/D Converter

- Fast ADC input clock
- Integrated PGA with gain 1x, 2x, 4x
- Support multi-trigger operation

Channel Select
Single Ended or Differential

Gain Setting
X1, x2, x4

MUX

PGA

V+12Bit
ADC

RESULT MUX

Zero Crossing Logic

HIGH LIMIT

LOW LIMIT

8x
Above

8x
Below

16x

12x

ADC RESULT

ADC OFFSET

8x

IRQ Logic

IRQ

External Use | 50
ADC Sampling helps to filter the measured current - anti-aliasing.
- Noise free ADC sampling when the power switch is not acting
- ADC sample is taken at middle of PWM pulse which is equal to average Current
  - But second phase samples are difficult to be located in middle of PWM Pulse
- Example Irregular Triggers

- Trigger 0 (T0) starts 1st conversion which ADC takes two conversions then wait next trigger
- Trigger 1 (T1) starts 2nd conversion which ADC takes one conversion then wait next trigger
- Trigger 2 (T2) starts 3rd conversion which ADC takes three conversions then generates INT
Irregular Triggers

Control Module
Sample Disable Register
Sample DISn ... Sample DIS1 Sample DIS0

ADC Scan Controller
Sample SCn Sample SC1 Sample SC0

ADC Scan Control register
Channel List (Select) Registers
Sample n ... Sample 1 Sample 0

ADC Start Signal T0, T1, T2, ...

Comparators
Programmable Delay Module
Transistor Power Stage
Motor or other Loads

Timers
Trigger Selector
PWM
Energy Source

ADC Module
Sample Result
Register Address
ADC Conversion Result
ADC Trigger
ADC Analog Input

Sample (0) Result
Sample (1) Result
Sample (2) Result
Sample (n) Result

Sample DISn ...
Sample DIS1 Sample DIS0

Sample SCn Sample SC1 Sample SC0

Sample n ...
Sample 1 Sample 0

ADC Module
IN0
IN2
IN3
INn
1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF
3. 8 pF noise damping capacitor
4. C1 = 1.4 pF
5. S1 and S2 switch phases are non-overlapping and operate at the ADC clock frequency
6. Equivalent input impedance, when the input is selected = \( \frac{1}{(ADC \ Clock\ Rate) \times 1.4 \times 10^{-12}} + 100 \text{ohm} + 125 \text{ohm} \)
ADC Current Injection Circuit

ADC Inputs (Pin Group 3)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage (external reference)</td>
<td>$V_{ADIN}$</td>
<td></td>
<td>$V_{REFL}$</td>
</tr>
<tr>
<td>Input voltage (internal reference)</td>
<td>$V_{ADIN}$</td>
<td>$V_{SSA}$</td>
<td>$V_{DDA}$</td>
</tr>
<tr>
<td>Input leakage</td>
<td>$I_{IA}$</td>
<td>$V_{REFH}$</td>
<td>$V_{REFH}$</td>
</tr>
<tr>
<td>$V_{REFH}$ current</td>
<td>$I_{V_{REFH}}$</td>
<td></td>
<td>$I_{V_{REFH}}$</td>
</tr>
<tr>
<td>Input injection current, per pin</td>
<td>$I_{ADI}$</td>
<td></td>
<td>$I_{ADI}$</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>$C_{ADI}$</td>
<td></td>
<td>See Figure 10-17</td>
</tr>
<tr>
<td>Input impedance</td>
<td>$X_{IN}$</td>
<td></td>
<td>See Figure 10-17</td>
</tr>
</tbody>
</table>
DC -Bus Voltage Sensing Circuit

Close to ADC pin as possible
Design Considerations for ADC

• Assure clean power supply and reference source to improve ADC conversion precision
• Use software calibration routine for ADC to improve ADC conversion precision
• Simultaneous sampling mode increases sample rate of ADC and keeps conversion synchronization for two different analog signals
• High input impedance to remove follower requirement
• Build-in clamp circuit to protect ADC from damaging by over-voltage
• Build-in PGA to improve dynamic precision of ADC conversion
Application Case for ADC

When time-division sampling is required?

Scan control mode helps reduce software overhead.
Digital to Analog Converters

- 12-bit Resolution
- Up to Two independent voltage mode DACs
- 2μs settling time settling time when output swing from rail to rail at 3KΩ/400pf load
- Output glitch filter to eliminate switching glitches
- Two output update modes
  - Asynchronous – Update On-demand
  - Synchronous – Update based on PIT or Timer Overflow, or PWM synch signal
- Automatic waveform generation generates square, triangle and sawtooth waveforms with programmable period, update rate, and range
- Software controlled power down mode
Quad Timer – All DSCs

- Unique architecture with - 2x Inputs (Primary + Secondary) and 1x Output
- Powerful MUX - Primary Input, Secondary Input and Output can be connected to external pins
- Individual channel capability - Input capture trigger, Output compare, Clock source, Prescaler
- Counters are pre-loadable, Count once or repeatedly
- Master Operation - any channel can be a master that broadcasts its compare signal to the other channels. Such way they can be configured to reinitialize their counters and/or force their OFLAG output signals to predetermined values.
- Compare - The TMRCMP1/2 registers provide the compare values (up/down) for the counter. If a match occurs, the OFLAG signal can be set, cleared, or toggled (polarity is selectable). If enabled, an interrupt is generated, and the new compare value is loaded into TMRCMP1 or 2 registers from TMRCMPLD1 and 2 (as enabled).
- Capture register stores a copy of the counter's value when an input edge (positive, negative, or both) is detected. Once a capture event occurs, no further updating of the Capture register will occur until the Input Edge Flag is cleared.
Quad Timer Operating Modes

Stop Mode - Counter is inert. No counting will occur

Edge Count Mode – Counts rising and falling edges (counting of simple encoder wheel)

Signed Count Mode – Counts primary input up or down based on polarity of secondary input

Count Mode – Counts rising or falling edges (generating periodic interrupts, timing purposes)

Gated Count Mode - Counts primary input if secondary input is high (signal width measurement)

Signed Count Mode – Counts primary input up or down based on polarity of secondary input

Cascaded Count Mode - Input is connected to the output of another (Great for large counts up to $2^{64}$)
Quad Timer Operating Modes

**Triggered Count Mode** – Start/Stop count of Primary input on rising edge of Secondary input.

*Diagram shows the timing relationship between Primary, Secondary, Count, and Timer_Out signals.*

**One-Shot Mode** - Provides timing delays
(ADC acquisition of new samples until a specified period of time has passed since the PWM sync signal occurred)

*Diagram shows the timing relationship between Primary, Secondary, Count, and Timer_Out signals with Timer_Out Assertion Count = CMP1 + 1.*

LOAD = 0, CMP1 = 4
Quad Timer Operating Modes

Fixed Frequency PWM - Fixed frequency, variable duty cycle (driving PWM amplifiers)

Variable Frequency PWM - Variable frequency and duty cycle (driving PWM amplifiers)

Adjustable Duty Cycle

Fixed Period

Adjustable Period

Pulse Output Mode - Supports stepper motor systems and provides change of signal frequency and number of pulses

Quadrature Count Mode
- Counter will decode the primary and secondary external inputs as quadrature encoded signals
- Compare interrupts will signal commutation

Count Mode

Primary Count

Output

Timer stopped due to Compare (COMP1 = 4)
Inter-Module CrossBar Module Capability

Reprogrammable interconnection among control peripherals to improve system flexibility and simplify system design.
AND-OR-INVERT Module

AND-OR-INT Output =

\[(0, A, \neg A, 1) \land (0, B, \neg B, 1) \land (0, C, \neg C, 1) \land (0, D, \neg D, 1) \] // product term 0

\[(0, A, \neg A, 1) \land (0, B, \neg B, 1) \land (0, C, \neg C, 1) \land (0, D, \neg D, 1) \] // product term 1

\[(0, A, \neg A, 1) \land (0, B, \neg B, 1) \land (0, C, \neg C, 1) \land (0, D, \neg D, 1) \] // product term 2

\[(0, A, \neg A, 1) \land (0, B, \neg B, 1) \land (0, C, \neg C, 1) \land (0, D, \neg D, 1) \] // product term 3

• AOI Input Mux Configuration Register

• Boolean Function Evaluation Configuration Register
And-OR-Invert Schematic
Configuration Examples for the Boolean Function Evaluation

- **AND-OR-INT Output =**
  - \((PT0\_AC[0] \& A | PT0\_AC[1] \& \sim A) \& (PT0\_BC[0] \& B | PTO\_BC[1] \& \sim B)\)  // product term 0
  - \((PT1\_AC[0] \& A | PT1\_AC[1] \& \sim A) \& (PT1\_BC[0] \& B | PT1\_BC[1] \& \sim B)\)  // product term 1
  - \((PT3\_AC[0] \& A | PT3\_AC[1] \& \sim A) \& (PT3\_BC[0] \& B | PT3\_BC[1] \& \sim B)\)  // product term 3

<table>
<thead>
<tr>
<th>Event Output Expression</th>
<th>PT0</th>
<th>PT1</th>
<th>PT2</th>
<th>PT3</th>
</tr>
</thead>
<tbody>
<tr>
<td>A &amp; B</td>
<td>A &amp; B</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>A &amp; B &amp; C</td>
<td>A &amp; B &amp; C</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(A &amp; B &amp; C) + D</td>
<td>A &amp; B &amp; C</td>
<td>D</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>A + B + C + D</td>
<td>A</td>
<td>B</td>
<td>C</td>
<td>D</td>
</tr>
<tr>
<td>(A &amp; ~B) + (~A &amp; B)</td>
<td>A &amp; ~B</td>
<td>~A &amp; B</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Peripherals to Trigger DMA Transfer

- eFlexPWM
- Timers
- A/D
- SCI
- I2C
- SPI
- Crossbar

Triggers (initiate DMA transfers)

Source

DMA Data transfers

Destination
Inter-Module CrossBar to Trigger DMA Transfer

Interrupt Request

Triggers (initiate DMA transfers)

eFlexPWM
COMPARATOR
PWM
Timer
I/O
RTC
PDB

Crossbar

Source

DMA transfers

Destination
LLC Resonant Converter with Sync Rectifier

Diagram showing the electrical components and connections of a LLC resonant converter with a sync rectifier. The diagram includes capacitors (C1, C2), inductors (Lr, Lm), transistors (T1, T2, T3, T4), and other components like PWM_A_0A/0B, XBar, CMPA/B, and ADC. The MC56F84xxx microcontroller is also depicted with connections for PWM frequency and voltage regulator.
Peak Current Controlled Phase-Shift Full-Bridge

Voltage Regulator → DAC → CMP → Digital PWM Module → PSFB

- Phase shift Compensation
- Sync
- Fault
- Inductor Current Feedback
- Voltage Feedback

MC56F82xx/84xxx
Executive Summary

Introduction

- Digital Power Control is the replacement of analog components to digital components within power control systems. Analog systems have many disadvantages that can be overcome by replacing with digital components and digital components can also bring many other advantages, such as greater control within the system and the ability to reduce reliability fluctuations.

Trends / Drivers

- Improve system flexibility—change quickly to meet market needs
- Improve systems efficiency—reduce system heat output
- Improve control—more accuracy, due to tighter system controls
- Reduce manufacturing costs—single design for product family, lower component count
- Reducing systems size, smaller chassis, smaller power supply needed

Technology

- High-resolution PWM, high speed analog-to-digital converter, digital signal process core, programmable gain amplifiers (PGA), on-chip comparators
- Enablement:
  - Soft Switching technique
  - Multiple-Phase interleaving Power Factor Correction
  - Adaptive close loop control
Resonant Converters
Introduction
Switch Mode Power Supply Introduction

- We can distinguish SMPS according many parameters:
  - Type of source
    - Voltage Source Converters, Current source Converters
  - Type of conversion
    - DC/DC, AC/DC, AC/AC or DC/AC
  - Ratio $V_{OUT}/V_{IN}$
    - Step Up, Step Down or Both
  - Galvanic Isolation
    - Isolated/non-isolated
  - Type of operation
    - Pulse with modulated, Frequency Controlled (Resonant)
Switch Mode Power Supply Introduction

• We can distinguish SMPS according many parameters:
  - Type of source
    ▪ Voltage Source Converters, Current source Converters
  - Type of conversion
    ▪ DC/DC, AC/DC, AC/AC or DC/AC
  - Ratio $V_{OUT}/V_{IN}$
    ▪ Step Up, Step Down or Both
  - Galvanic Isolation
    ▪ Isolated/non-isolated
  - Type of operation
    ▪ Pulse with modulated, Frequency Controlled (Resonant)
PWM Operated Switch Mode Power Supply

- The semiconductor switches generate square wave voltage output using PWM modulation - Vg
- The Vg is rectified by output rectifier and filtered by a low pass filter
- The Vo corresponds to actual duty cycle

+ Simple design
- Higher switching looses
- Lower switching frequencies – bulky components
=> Resonant converters
Resonant Converter Introduction

- The resonant converter employs **resonant circuit** between semiconductor switches and rectifier.
- The **resonant circuit** consist of at least one capacitor and inductor.
Resonant Converters

- There are many variants, how to implement resonant circuit (two and three components)
- This presentation focuses on widely used combinations:
  - Series resonant converter
  - Parallel resonant converter
  - LLC Resonant converter

All possibilities for two components resonant circuit
Resonant Converter Introduction

- The resonant tank impedance is frequency dependent
- Series LC (RLC) circuit features at resonant frequency $f_r$
  - The resonant tank has minimal impedance
  - There is zero voltage drop on resonant tank (ideally)
  - The voltage on resonant circuit components can be higher than the input voltage

\[
f_r = \frac{1}{2\pi \sqrt{LC}}
\]
Resonant Converter Introduction

- Zero Voltage Switching (ZVS) of MOSFET transistor
  - The MOSFET transistor is switch on at zero drain-source voltage
  - There are no turn on losses
Resonant Converter Introduction

- Series Resonant Converter
  - The resonant tank is connected in series with the load $R_L$
Resonant Converter Introduction

• Series Resonant Converter
  - The resonant tank is connected in series with the load $R_L$
  - The resonant tank creates voltage divider together with the load
Resonant Converter Introduction

• Series Resonant Converter
  - The resonant tank creates voltage divider together with the load
  - The resonant tank impedance is frequency dependent

\[ V_O = Gain \times V_G \]
Resonant Converter Introduction

• Series Resonant Converter (SRC) - Summary
  - The SRC can run at ZVS over the resonant frequency
  - At light loads it is difficult to control output voltage
  - High conduction losses at high input voltage and light loads
Resonant Converter Introduction

- Parallel Resonant Converter
  - The load $R_L$ is connected in parallel to resonant circuit
Resonant Converter Introduction

• Parallel Resonant Converter

\[ V_o = \text{Gain} \times V_G \]
Resonant Converter Introduction

• Parallel Resonant Converter (PRC) - Summary
  - The PRC can also run at ZVS over the resonant frequency
  - The PRC can work at no load condition
  - High conduction losses at high input voltage and light loads
Resonant Converter Introduction

• LLC resonant Converter
  – Additional inductance is employed in resonant circuit
  – The load $R_L$ is connected in parallel to this inductance
Resonant Converter Introduction

• LLC resonant Converter
  - When transformer used in LLC converter, the magnetizing inductance and leakage inductance can be used in resonant circuit instead of external separate inductances
  - This is one of the advantages of LLC resonant converter
Resonant Converter Introduction

• LLC Resonant Converter
  – There are two resonant frequencies: first one for $L_r$ and $C_r$ and second one for $(L_r + L_m)$ and $C_r$

\[ V_O = \text{Gain} \times V_G \]
Resonant Converter Introduction

- LLC Resonant Converter – Operation at no Load
Resonant Converter Introduction

- LLC Resonant Converter – Operation at Resonance
Resonant Converter Introduction

- LLC Resonant Converter – Operation below Resonance
Resonant Converter Introduction

- LLC Resonant Converter – Operation above Resonance
Resonant Converter Introduction

• LLC Resonant Converter - Summary
  - The LLC resonant converter can run at ZVS in whole range of the operating frequency (above even below resonant frequency)
  - The LLC resonant converter can work at no load condition. The turn of current can be controlled by Lm inductor
  - The LLC resonant converter works at resonant frequency at nominal input voltage
  - The LLC resonant converter can operate over wide range of operating input voltage
Resonant Converter Introduction

- Resonant Converter Comparison

<table>
<thead>
<tr>
<th></th>
<th>SRC</th>
<th>PRC</th>
<th>LLC</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZVS Operation</td>
<td>Above $f_r$ only</td>
<td>Above $f_r$ only</td>
<td>Yes</td>
</tr>
<tr>
<td>Operation without load</td>
<td>No</td>
<td>Yes, but high losses</td>
<td>Yes</td>
</tr>
<tr>
<td>Operation at $f_r$</td>
<td>No (Close to $f_r$)</td>
<td>No (Close to $f_r$)</td>
<td>Yes</td>
</tr>
<tr>
<td>Operation at wide input voltage range</td>
<td>No, High losses</td>
<td>No, high losses</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Resonant Converter Introduction

- Operation at wide input range
  - There is a requirement, that power supply must delivery output power during one whole period, if there is mains line drop out
Resonant Converter Introduction

- Operation at wide input range – PWM modulated Converters
  - The PWM modulated converters are not able to increase gain by changing duty cycle. Therefore the $V_{BUS} - V_{min}$ has to be small (20-30V).
  - The whole energy has to be stored in the DC bus capacitor.

- Example of DC bus capacitor calculation

\[
P_{out} = 500W \\
V_{BUS} = 400V \\
V_{min} = 370V \\
f_{min} = 45Hz
\]

\[
C \geq \frac{2P}{f_{min}(V_{BUS} - V_{min})} = 962\mu F
\]
Resonant Converter Introduction

• Operation at wide input range – Resonant Converters
  - Some resonant converters can increase gain over 1 by changing switching frequency. Therefore the $V_{BUS} - V_{min}$ can be much higher than for PWM modulated converters.

  - Example of DC bus capacitor calculation

\[
P_{out} = 500W \\
V_{BUS} = 400V \\
V_{min} = 200V \\
f_{min} = 45Hz \\
C \geq \frac{2P}{f_{min}(V_{BUS} - V_{min})} = 185 \mu F
\]

- The DC Bus capacitor can be significantly smaller 185 $\mu F$ versus 962 $\mu F$!!!
Application Example: Digital Control of LLC Resonant Converter
Digital Control of LLC Resonant Converter

• General requirements
  - Powerful Core
    ▪ The control loop is calculated every 5-20 $\mu$s (motor control application 50 – 200 $\mu$s)
  - Very fast A/D Converter (better than 1$\mu$s conversion, capable of parallel conversion)
  - PWM module capable of high resolution frequency and duty cycle generation
    ▪ The resolution should be comparable to resolution of ADC measurement
    ▪ It means more than 10 bits for frequencies 100 – 400 kHz

- Search in Freescale portfolio leads to DSC 56F824x/5x
  ▪ These devices meet the best the requirements mentioned above
LLC Resonant Converter – Freescale Solution Overview

• Used SMPS Topology
  – Primary Side: Two Phase Interleaved PFC (Average Current Control)
  – Secondary Side: Half Bridge LLC Resonant Converter with Synchronous Rectification for 12V output
  – Additional Synchronous Buck Converter for 5V output

• Fully Digital Control by Two DSCs:
  – Primary Side: MC56F8013
  – Secondary Side: MC56F8257
Freescale LLC Resonant Converter - Detail Parameters

• Input voltage
  - 85-265Vac @ 45-65Hz

• Output voltage
  - 12V/41 Amps (max.)
  - 5V/25 Amps (max.)

• Output Power
  - 500W shared by both voltage outputs. The power limit can be set individually by SW for each voltage output.

• Communication
  - PM Bus communication (HW ready)
  - CAN Communication (HW ready)
  - Communication with PC using USB

• Full Fault Protection
  - Over-voltage, Over-current, over-temperature on both primary and secondary side. Active controlled cooling
Freescale LLC Resonant Converter - Block Diagram

AC/DC

DC/DC

3xADC

2xPWM

MC56F8013

HV daughter card

DC-Bus 400V

Isolation barrier

2xPWM

Isolation

2xADC

MC56F82xx

HV daughter card

SCI

SCI1

DC-Bus

12V

3,3V

12V

3,3V

SCI2

Auxiliary Power Supply

12V

5V

12V

85-265V
45-65Hz

12V

PM – Bus

CAN

SCI/USB

Host PC

SCI

SCI1

I2C

CAN – Bus
Freescale LLC Resonant Converter - Primary Side

• PFC Topology
  – Two Phase Interleaved Boost Converter
• PFC Control Algorithm
  – Fully Digital Average Current Control by DSC MC56F8013
• Measured Quantities
  – Input Rectified Voltage
  – Input Current
  – DC Bus Voltage
  – Heatsing Temperature
• Generated signals
  – 2x PWM signals for MOSFETs transistor (100kHz)
  – 1x PWM signal for cooling fan
  – 1x GPIO input relay control
• Fault Protection
  – HW over-current protection
  – SW over-voltage/under-voltage protection
  – SW over-temperature protection
Freescale LLC Resonant Converter - PFC Schematic

8 kondu na dc bus 18x31,5mm 56uF/450V
Freescale LLC Resonant Converter - PFC SW Implementation

• Inner current loop
  – PI Controller running every 10 μs

• Outer voltage Loop
  – PI Controller with running every 500 μs
  – Optionally output power feedforward (sent from secondary side)

• Other Control Tasks
  – Cooling fan control based on heatsing temperature
  – Input relay control
  – Communication with secondary controller
Freescale LLC Resonant Converter - Secondary Side

• Main Converter Topology (12V Output)
  - Half Bridge LLC Resonant Converter with synchronous rectification
• Secondary Converter Topology (5V Output)
  - Synchronous Buck Converter
• Control Algorithm
  - Fully Digital Voltage Mode Control by DSC MC56F8257 for both converters
• Measured Quantities
  - 2x Output Voltage
  - 2x Output Current
  - Secondary Side PCB Temperature
• Generated Signals
  - 2x PWM signals for half bridge MOSFET transistors (50% duty cycle, 100kHz – 400kHz)
  - 2x PWM signals for synchronous rectification MOSFET transistors (50% duty cycle, 100kHz – 400kHz)
  - 2x PWM signals for secondary buck MOSFET transistors (500 kHz)
• Fault Protection
  - 2x HW over-current protection
  - 2x SW over-voltage protection
  - Over-temperature protection
Freescale LLC Resonant Converter - LLC Converter Schematic
Freescale LLC Resonant Converter - Buck Converter Schematic
Freescale LLC Resonant Converter - Secondary Side SW Implementation

- LLC Resonant Converter
  - PI Controller running every 10 ms
- Buck Converter
  - PID Controller running every 10 ms
- Other task Control
  - Communication with host PC
  - Communication with primary controller
  - Communication via PM Bus (Optional)
  - Communication via CAN (Optional)
Freescale LLC Resonant Converter - Aux. SMPS

- Auxiliary power supply to power all circuits on both primary and secondary side
- Topology: Flyback Converter
- Independent control by dedicated IC (TNY275)
- Output voltage: 12V/3.3V
- Output power: 8W
Freescale LLC Resonant Converter - Aux. SMPS Schematic
Freescale LLC Resonant Converter – Picture Gallery