Semiconductor 101: Functionality and Manufacturing of Integrated Circuits

AMF-ENT-T0194

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Field Engineer
Agenda

• What are Semiconductor Devices?
• How Semiconductors are Made
  – Front-End Process
  – Back-End Process
• Fabrication Facility and Equipment Issues
• Business Aspects of Supplying Semiconductors
Semiconductor Terms and Acronyms

FET

Digital

Microprocessor

(N,P,C)MOS

Transistor

Analog

Semiconductor

Silicon

Microcontroller
A conductor carries electricity like a pipe carries water.

A semiconductor controls the flow of electricity like a faucet controls water.

An insulator stops the flow of electricity like a plug blocks water.
Semiconductor Basics

- Copper, a conductor, has one electron per atom available for conduction.

- A useful semiconductor requires about 10 orders of magnitude less

- This means adding one doping atom in a billion

- Impurities have to be below one in 10 billion

n Type doped with P or As

p Type doped with B
Basic IC Building Block: MOSFET

- A MOSFET transistor is nothing more than a voltage controlled switch!
- A transistor is just like a light switch on a wall, except that a voltage is used to turn the switch on and off instead of a lever.
- A good analogy to a transistor is two lakes connected by a canal.

![Diagram of two lakes connected by a canal with a "flood gate" regulating the flow of water.]

- The "flood gate" regulates the flow of water between the two lakes (source and drain).
- A real transistor switches the flow of electric current on and off instead of water.
N-Channel MOSFET Operation

- Current (water) will not flow from an n-type reservoir to a p-type region because it would have to flow \textit{uphill}.

- Only way we can get water from one p-type reservoir to another is by way of a \textit{n-type channel}.

- By using a capacitor and applying a positive voltage to that capacitor, we can change the apparent conductivity of the channel from p to n and turn the transistor on.

- In reality, the drain is usually at a lower elevation than the source so the water will flow downhill to the drain.
Anatomy of a MOSFET: Cross-Section

- A MOS transistor is nothing more than a voltage-controlled switch.
- A MOS transistor is really just a capacitor with two extra terminals.
Anatomy of a MOSFET: Top View

Capacitor

Isolation (oxide)

source
drain

Top View
How a CMOS Inverter Works

- PMOS: Normally ON
- NMOS: Normally OFF

<table>
<thead>
<tr>
<th>IN</th>
<th>Logic</th>
<th>OUT</th>
<th>Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>0</td>
<td>~Vdd</td>
<td>1</td>
</tr>
<tr>
<td>Vdd</td>
<td>1</td>
<td>0V</td>
<td>0</td>
</tr>
</tbody>
</table>
Semiconductor Device Types

• **Analog** semiconductor devices deal in precise electric properties, most commonly voltages. Transistors within the device are designed to measure and manipulate these properties. Analog devices are well suited to processing real-world signals, as electronic patterns are used to directly represent the original.

• **Digital** devices do not deal in the values of actual voltages; rather, they simply detect the presence or absence of a voltage. The presence of a voltage is represented digitally as a “1,” with the absence represented as a “0.” These 1s and 0s can be processed and manipulated digitally with great flexibility.

• **Mixed Signal** – These devices include both analog *and* digital circuitry. Mixed signal devices are difficult to design and build, but bring the benefits of both analog and digital processing together.
Device Types: Semiconductor Industry Association (SIA) Framework

- **Discretes, Optoelectronics, Sensors** – Includes all non-integrated circuit semiconductor devices. A discrete is a single transistor in a package. Sensors are discrete devices that measure real-world input. Optoelectronics are discrete devices that produce or measure light.

- **Analog** – Devices used to process real-world signals using electronic voltage patterns that represent the original. Includes SLICs (standard linear components) and ASSPs (application-specific analog ICs).

- **Microcomponents** – All digital processors, including microprocessors (MPUs), microcontrollers (MCUs) and digital signal processors (DSPs).

- **Logic** – All non-microcomponent digital logic. Includes ASICs (custom logic), ASSPs (standard specialty logic products), FPGAs (programmable logic), display drivers and general purpose logic.

- **Memory** – Memory devices are used to store data either for short periods of time or permanently. Includes volatile (DRAM, SRAM) and non-volatile (flash, ROM) memory.
Microcomponents in Detail

**Microcomponents**: Devices designed to perform intensive compute processing and system control

**Three Key Types:**

- **Microprocessors** – digital processors that execute instructions and perform system control functions. MPUs are optimized for general purpose data processing

- **Microcontrollers** – stand-alone devices that perform embedded compute functions within an overall system. MCUs contain single or multiple processing elements as well as on-chip, RAM, ROM, and I/O logic.

- **Digital Signal Processors** – specialized high speed programmable processors designed to perform real-time processing of digital signals
## Packaging Options for Mixed-Signal Functions

<table>
<thead>
<tr>
<th>Semi-Discrete Solution</th>
<th>Multi-die SiP</th>
<th>Monolithic SiP</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Standard MCU</td>
<td>• Single package</td>
<td>• MCU and Analog on the same die</td>
</tr>
<tr>
<td>• Application Specific Analog IC (ASIC)</td>
<td>• Die-to-die bonding</td>
<td></td>
</tr>
</tbody>
</table>

![Semi-Discrete Solution Image](image1.png)

![Multi-die SiP Image](image2.png)

![Monolithic SiP Image](image3.png)
Example of Inertial Sensing Elements

Z axis Elements

Poly Silicon, Folded Beam Z-Axis Sensing

X axis Elements

Poly Silicon, Interdigitated X and XY-Axis Sensing

Harmems, Interdigitated X and XY Sensing
Multi-Die Packaging for Sensors - QFN Package

Automotive Qualified Package:
In production since 2006

Wire bonds
ASIC
Lead Frame
g-cell device
g-cell cap

1.98mm
6 mm
Accelerometer Device Images

- G-Cell Die
- ASIC Die
- Mold Compound
Application Example: Body Control Module

- Door Lock
- H-bridge
- Watchdog
- MCU S08
- Warning LEDs
- Various sensor inputs
- System Basis Chip
- SBC
- CAN
- Transceiver
- Multiplexer
- MSDI
- Various sensor inputs
- LIN Transeiver
- Multiplexer
- MSDI
- Various sensor inputs
- MCU MPC5xxx / S12x
- Timer
- PWM
- ADC
- Real Time Clock
- Various sensor inputs
- CAN
- CAN Transeiver
- CAN Transeiver
- Multiplexer
- MSDI
- Multiplexer
- MSDI
- UHF Transceiver MC33696
- Amplifier
- Internal Lighting
- Horn
- External lighting
- LED control
- Seat control
- Various Outputs
- High-side e-switches
- Low-side switches
- LED Drivers COSS
- Antenna

Various sensor inputs

Internal Lighting

Horn

External lighting

LED control

Seat control

Various Outputs

21
Control Modules – Functional Breakdown

- Compute Engine
- Analog Signal Conditioning
- Low Voltage Core/NVM
- Power Drivers
- Protection
- High Voltage
- Peripherals interface to the real world

Mother Nature

Peripherals interface to the real world
Example Die Photos of Integrated Circuits
MPC561 Die Photo

- 32-bit MCU with Power Architecture® CPU core
- Die size = .55 cm²
- 5 million transistors
- 16 million vias and local interconnects
- 2 polysilicon layers
- 3 aluminum metal layers
- 0.25 μm technology
MPC5554 Floor Plan

- Red – CPU
- Blue – ETPU
- Green – EQADC
- Purple – DSPI
- Yellow – EMIOS
- Orange – FlexCAN
- White – EBI
- Dark Green – SIU
- Magenta – JTAG
- Grey – SCI
Freescale ATMC C90FG Technology Highlights

- ~350 process steps, 55 mask layers
- ~75 million transistors
- ~400 to 1,600 chips per 200 mm wafer
- Embedded ADC, SRAM, non-volatile memory

6 Layers of Cu Metal
1.15 um² SRAM Bitcell Array

NVM Bitcell Array
NVM Bitcell
Logic

State-of-the-art Power Architecture®
32-bit MCU engine control
600+ DMIPS – MPC5674F
What Is a Micron Between Friends?

- 0.5 micron is \( 1/200^{th} \) the width of a human hair

1997 mainstream process

- 55 nm is \( 1/2000^{th} \) the width of a human hair

2013 mainstream process

Electron microscope photograph of a common Texas fire-ant eye
Design Rules

• The fab-provided Design Rule Manual (DRM) is an important way that the semiconductor fab communicates with the IC Design team

• Over 500 pages of design rules

• Typical contents include:
  − Technology overview
  − Physical Layout Rules
  − Electrical specifications
  − Reliability
DRM Technology Overview

• Approved voltages, temperatures, etc
• Process Options
  − Individual device offerings
  − Allowed / forbidden device combinations
  − Metallization options
• Main process features
  − Brief process flow
## DRM Physical Layout Rules Example

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Active-poly distance</td>
<td>&gt;0.05um</td>
</tr>
<tr>
<td>B</td>
<td>Active-poly corner</td>
<td>&gt;0.1um</td>
</tr>
<tr>
<td>D</td>
<td>Active overlap poly</td>
<td>&gt;0.16um</td>
</tr>
</tbody>
</table>
Design Rules

Figure 3 Isolation and Polysilicon Layout Rule

Table 13 Polysilicon and Isolation Layout Recommendations

<table>
<thead>
<tr>
<th>Recommendation</th>
<th>Description</th>
<th>Design (um)</th>
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<tbody>
<tr>
<td>104R</td>
<td>POLY space to POLY (over ACTIVE - for lower silicide resistance).</td>
<td>≥ 1.30</td>
</tr>
<tr>
<td>113R</td>
<td>POLY space to ACTIVE (for low POLY wiring capacitance)</td>
<td>≥ 0.30</td>
</tr>
<tr>
<td>114R</td>
<td>POLY space to ACTIVE corner, for constant FET W_{eff}</td>
<td>≥ 0.50</td>
</tr>
<tr>
<td>115aR</td>
<td>POLY corner space to ACTIVE for maximum Loff control, (gate corner and ACTIVE are on same FET)</td>
<td>≥ 0.50</td>
</tr>
<tr>
<td>132R</td>
<td>POLY maximum area (um²) (POLY that intersects ACTIVE only)</td>
<td>≤ 500</td>
</tr>
</tbody>
</table>
Semiconductor Terms and Acronyms: Review

FET
Micron
(N,P,C)MOS
Transistor
Digital
Analog
Semiconductor
Silicon
Microcontroller
Integrated Circuit Manufacturing Process
IC manufacturing uses a recursive deposition and masking process to define patterns of doped areas, isolation films and metal conductors to create solid state devices.

Diffusion grows or deposits a layer of oxide, nitride, poly or similar material.

Photo spins on photoresist, aligns reticle and exposes wafer with reticle pattern. Develop removes resist from exposed areas.

Etch removes film layer that was uncovered during develop. Strips resist.

Implant dopants are implanted for electrical characteristics.

Metals/Films connects devices electrically and isolates circuit pathways.

CMP polishing technique to keep surfaces flat so more layers can be added.

Probe/Test test device functions.
Anatomy of a MOSFET: Cross-Section

- A MOS transistor is nothing more than a voltage-controlled switch.
- A MOS transistor is really just a capacitor with two extra terminals.
Preparation for Use in Integrated Circuits

- Silicon is the second most abundant element on earth after oxygen (25% of crust)

**Purification operations**

\[ \text{SiO}_2 + C \rightarrow \text{Si} + \text{CO}_2 \]

1900°C Furnace gives metallurgical grade Si

\[ \text{Si} + 3\text{HCl} \rightarrow \text{SiHCL}_3 + \text{H}_2 \]

Refining to reduce impurities

\[ \text{SiHCL}_3 + \text{H}_2 \rightarrow \text{Si} + 3\text{HCl} \]

The white sand of Abel Tasman’s beaches in New Zealand’s South Island is a typical source of silicon dioxide.
Making an Ingot

- A pure silicon seed crystal is placed into a molten sand bath.
- This crystal will be pulled out slowly as it is rotated (1 mm per hour).
- The result is a pure silicon cylinder that is called an *ingot*. 
Examples of a Completed Ingots

- Single crystal silicon ingot length: 110 cm

200mm Silicon Ingot
Preparing the Wafers

- The ingot is ground into the correct diameter for the wafers.
- Then, it is sliced into very thin wafers.
- This is usually done with a diamond saw.

Slicing : 640μ thick
Next, the wafers are polished in a series of combination chemical and mechanical polish processes.
Mask-Making Process

The Process

- Start with ultra-pure glass plates with a surface deposition of chromium.
- Computer generated layouts of the IC drive a laser beam or electron beam to selectively remove chromium and create the mask or reticle.

Design Driven

- Increased complexity
- Long write times
- New product acceleration
Small Geometries: Stretching the Wavelength

No OPC

With OPC

Optical Proximity Correction (OPC)

Mask

Printed

Phase Shift Mask

Mask

Printed

Quartz recess

Chrome

Resist
Epitaxy

- Growth of an ultra pure layer of crystalline silicon

- Approximately 3% of the wafer thickness

- Contaminant-free for the subsequent construction of transistors
Photolithography Process

- The wafer is coated with photoresist material.
- The reticle containing a layer’s image of one or more die are exposed by a light source through a lens system onto the wafer.
- The wafer is then stepped over to the next die and the process repeated until the wafer is completely exposed.

All processing done on a wafer lot basis.
Lithography Process Overview

Substrate with Thin Film

Resist Coat and Post Apply Bake (PAB)

Expose Resist

Post Exposure Bake (PEB)

Develop Resist

Etch
Oxidation and Exposure

• The epi-wafer is exposed to high temperature to grow an oxide layer.

• A layer of photoresist is spun onto the oxide.

• The stepper exposes the pattern onto the photoresist.

• The photoresist is then developed to leave the pattern on the wafer.
Adding Photoresist

- Dispenses
- Wafers receivers
- Hot plate
- Control keyboard
- Track 1
- Track 2
Exposure

- Mercury Lamp
- Shutter
- Reticle
- Lens
- Wafer Stage
- Reticles Storage
- Wafer Loading/Unloading
Etch and Strip

- An etch process (wet or dry) is used to remove the oxide where the photoresist pattern is absent.

- The photoresist is then stripped completely off the wafer, leaving the oxide pattern on the wafer.
Etching (Chemical and Reactive Ion)

- Exhaust management
- Process control
- Heating element
- Acid waste
- Drain
- Process gases
- Radio frequency power supply
- Wafers with resist
- Ionized Gas
- ETCH
- Vacuum system
- Process chamber under vacuum
- Acid waste
- Drain
- QDR
- QDR
Diffusion and Implant

• The oxide acts as a barrier when dopant chemicals are deposited on the surface and diffused into the surface.

• Alternatively, dopants may be bombarded into the silicon surface via and ion implant beam.

• The induced ions create regions with different properties of the silicon semiconductor material.

• These regions become the source and drain of the CMOS transistor.
Diffusion Furnace

• Diffusion furnaces are classified as either horizontal or vertical.

• Vertical gives better process control and tends to be cleaner but takes up more space.

• Changing the process gases allow us to grow films (oxide, nitride, poly) or dope the wafers to change the electrical characteristics.

• They operate at temperatures generally between 650°C and 1200°C.

• Temperatures in furnaces are controlled to better than +/- 1°C.

• Furnaces can process 50-200 wafers per run depending on type of process.

• Process times can vary from 4-20 hours (thicker films take longer to grow/deposit).
Ion Implantation and Annealing
Typical Photo-Lithography Process

- oxidation
- optical mask
- photoresist removal (ashing)
- stepper exposure
- photoresist coating
- photoresist development
- spin, rinse, dry
- acid etch
- process step
Critical Cleaning

Process Conditions
Temperature: Piranha Strip is 180 degrees C.

RCA Clean
SC1 Clean (H₂O + NH₄OH + H₂O₂)
SC2 Clean (H₂O + HCl + H₂O₂)

Piranha Strip
H₂SO₄ + H₂O₂

Nitride Strip
H₃PO₄

Oxide Strip
HF + H₂O

Dry Strip
N₂O
O₂
CF₄ + O₂
O₃

Solvent Cleans
NMP
Proprietary Amines (liquid)

Dry Cleans
HF
O₂ Plasma
Alcohol + O₃
Using the same oxidation and photolithography process, an opening is made in the oxide to build the transistor’s gate region.

A thin gate oxide or silicon nitride is deposited via Chemical Vapor Deposition (CVD) process to act as an insulator between the gate and the silicon.

This is followed by Physical Vapor Deposition (PVD) or “sputtering” of a conductive polysilicon layer to form the transistor’s gate region.
Oxidation

- Various oxides are grown or deposited to insulate or protect the formed transistors.

- Deep Field Oxides are grown to isolate each transistor from its adjacent partners.

- Dielectric isolation oxides are deposited to insulate the transistors from the interconnecting layers that will be built above.

- Passivation oxides are later deposited on top of completed wafers to protect the surface from damage.
Interconnect: Vias

Using the same photolithography process, “via” contact holes are etched down to the three transistor regions that need to be connected to other components on the chip.
Interconnect: Metallization

- A layer of aluminum is deposited on the surface and down into the via holes.

- Excess aluminum is etched away after another photolithography process, leaving the desired interconnect pattern.

- Another layer of dielectric isolation oxide is deposited to insulate the first layer of aluminum from the next one.
Metal Deposition

A

B

C

Load-lock

1

2

3

4

Etch Chamber

Heating Chamber

Process Chamber

Aluminium Target

Gas: Argon

Al Sputtered

Vacuum Pump

NXP

freescale™
Why Do We Need CMP?

• Without CMP, the wafer will have a lot of topography (mountains and valleys).
• Excessive topography will:
  - Limit how small photo can print
  - Cause thinning of films on side walls
  - Compromise etch uniformity
  - Compromise film deposition uniformity
Process with CMP
Interconnect Layers

• Another set of via holes are etched in the dielectric isolation oxide to enable access down to the layer below.

• Contact plugs are deposited (often tungsten) into the vias to reach down and make contact to the lower layer.

• The next layer of aluminum is deposited, patterned and etched.

• This process is repeated for as many interconnect layers as are required for chip design.
This process requires more than 190 stages. Each stage contains multiple substeps.
Simple Surface Micromachining Process

1. Silicon substrate
2. Oxide growth
3. Oxide etching
4. Deposition of structural layer
5. Structural layer etching
6. Oxide removal
• Charge is placed on floating gate with hot carrier injection or Fowler Nordheim tunnelling

• Charge remains trapped on floating gate giving non volatile memory function
Class Probe

- Parametric testing of test structures
- Test structures in scribe lines between product die

SGPC = scribe grid process control

Not to scale (~0.1mm)
Typical Class Probe Structures

- Transistors
- Metal to metal linkage
- Contact chains
- Via chains
- Resistors
- Capacitors
- Gate Oxide

\[ \text{Diagram showing various probe pads and connections} \]
Background

- Wafer thickness is reduced from 640µ to 300µ
Semiconductor Fabrication Equipment
Freescale ATMC Factory Configuration

- **Process Level**: Work Zone Class 1, Utility Zone Class 100, Center Corridor, Work Zone Class 1, Utility Zone Class 100, Work Zone Class 1, Work Zone Class 1, Utility Zone Class 1, Work Zone Class 1, Work Zone Class 1.
- **Fan Deck**: HPM Rooms, Crawl Space, Electric Rooms, ULPA Ceiling, Process Level, Subfab.
- **Interstitial**: Maintenance Shops, Parts, Quartz, Wafer Storage.
- **Support Tools**: HPM Rooms, Crawl Space, Electric Rooms.
- **Piping**: HPM Rooms, Crawl Space, Electric Rooms.
NTMC Cleanroom: Systems, Controls, Airflow Infrastructure
ATMC Cleanroom Airflow Filtration

• First stage makeup air pre-filters are 30% efficient for 3-10um sized particles.

• Second stage makeup air pre-filters (inside makeup air units) are 95% efficient for 0.3-1µm sized particles.

• Final stage filters (cleanroom ceiling grid) are Ultra Low Penetrating Air (ULPA) filters that are 99.9995% efficient for 0.1um sized particles.

• 100% cleanroom ceiling ULPA filter coverage in work zone areas

• 40% filter coverage in utility zone areas

• Average laminar airflow velocity is 90-110 ft/min
Freescale CHD-Fab Macro Layout

North & South
- Analytical 8.3k sf
- Polymide 5.8k sf
- Probe 9k sf
- Lot Start Ship
- Cleans/ISD 2.5k sf
- Implant
- Diffusion/Cleans 10k sf
- Photo i-line 7k sf
- Implant
- Diffusion/Cleans 6.6k sf
- Implant Cleans
- CVD (TEOS, PAS) 5.6k sf
- Photo DUV 6.1k sf
- Implant
- ETCH 8.2k sf
- YE 2.5k sf
- Probe 9k sf
- East Module (Bldg “M”)
- Metals PVD 11 ksf
- Implant 23k sf
- Epi
- “A” Building to the East of “M” Building has additional 8k sqft of Probe
- Gown 2.1k sf
- Copper 3.5 ksf
- CMP 22k sf
- MRAM
- Probe 27k sf
Oak Hill Texas Fab Facts

• 85,000+ square feet of sub-class 1 clean room space supporting wafer capacity of 6,000 WPW

• Approximately 750 people working at OHT-Fab

• Factory operates 24 hours per day, 364 days per year

• Factory moves ~6,400,000 CFM, enough to fill 120 hot air balloons every minute

• 9,300 tons of refrigeration capacity, sufficient to cool 2,800 homes

• Factory uses 44,000,000 gallons of water/month, equivalent to 4,400 homes

• Factory uses ~215,000,000 KWH per year, equivalent to 6,000 homes

• Factory has more than 17 miles of stainless steel piping and more than 50 miles of electrical wiring
## 200MM Equipment List for .18 Micron Facility

<table>
<thead>
<tr>
<th>Equipment</th>
<th>Number</th>
<th>Price ($M)</th>
<th>Total ($M)</th>
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<tbody>
<tr>
<td>Chemical Vapor Deposition</td>
<td>24</td>
<td>3</td>
<td>60</td>
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<tr>
<td>Physical Vapor Deposition</td>
<td>23</td>
<td>4</td>
<td>81</td>
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<tr>
<td>Steppers</td>
<td>54</td>
<td>8</td>
<td>432</td>
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<tr>
<td>Photoresist Processing</td>
<td>54</td>
<td>2</td>
<td>108</td>
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<td>Etch</td>
<td>55</td>
<td>3</td>
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<td>Process Control</td>
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<tr>
<td>Miscellaneous</td>
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<td>-</td>
<td>67</td>
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<tr>
<td><strong>Total</strong></td>
<td></td>
<td></td>
<td><strong>1,126</strong></td>
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Wafer Costs vs. Masking Steps

![Image of graph showing the relationship between the number of masking steps and wafer costs for different micron sizes. The graph includes lines for 0.50 Micron, 0.35 Microns, 0.25 Microns, 0.18 Microns, 0.15 Microns, and 0.13 Microns.](image)

Source: ICE
Moore’s Law

Advancement towards finer lithography, which enables smaller and smaller transistors, is the primary driver behind the dramatic improvement in semiconductor device performance over the past few decades.

Moore’s Law states that the number of transistors on a chip doubles about every two years. The phenomenon was first noticed by Intel founder Gordon Moore, and has held basically true for the past 40 years or so.

In addition to the doubling of transistor density, each new lithography generation usually brings 0.7X minimum feature scaling, 1.5X faster transistor switching speed, reduced chip power, and reduced chip cost.
• Larger wafers = more die per wafer = lower cost per die
• 300mm (12”) wafers yield more than twice as many die for the same product as a 200mm (8”) wafer
Wafer Size Trends (2)

- First 450mm fab expected in Albany NanoTech Complex in 2013 followed by another in 2016

Source: Gartner March 2012

Semiconductor Capacity Trend by Wafer Size
Research and Development

- R&D provides two major benefits:
  - Increases productivity
  - Enhanced process capabilities (required to remain competitive)
Advanced Platform Technology Landscape

- Crolles2 Alliance advanced process spending is not competitive for the scope of technologies and options covered.
- Freescale must establish a cooperation model resourced at the appropriate level.

*based on Freescale and analysts estimates
The IBM Alliance

Increase partnership

- Low Power CMOS
- High Performance SOI
- CMOS LP / GP
- Packaging
- e-Non Volatile Memory
- RF CMOS
- Sensors
- SmartMOS Power & Analog
- GaN
- GaAs RF

Increase differentiation

HPSOI

- IBM
- AMD
- freescale™

LP-Bulk

- IBM
- SAMSUNG
- Chartered
- Infineon
- Toshiba
- freescale™

GaN

Research

AMD

SONY
Integrated Circuit Back-End Manufacturing Processes
Test and Assembly Process
Wafer Mount and Saw

**Wafer Mount Process Description**
Wafers are mounted on UV tape and carefully placed on the metal frame to ensure correct rotational alignment.

**Wafer Saw Process Description**
A mounted wafer is placed on a metal supporting plate under the mounting tape. Process parameters are set and the diamond blade cuts through the silicon wafer targeting 100% of the wafer depth.
Die Attach and Cure

Process Description
Epoxy is dispensed in the die flag area of the substrate in a specified pattern (usually star) followed by a pick and place process that removes the die from the tape carrier and places it over the dispensed epoxy.

Die Bond Cure Process
Substrates are placed in a nitrogen purged oven. During the cure time, the epoxy resin completes the cross linking process to form a rigid material. Nitrogen is used to replace the trapped air/moisture that may interfere with the cross linking process.
Plasma Clean and Wire Bond

Plasma Clean Process Description

Plasma clean is then used to remove contaminants from the die bond pad surface to improve wire bondability and adhesion. He/O2 and Ar/H2 are two common gas mixtures that are used. Ar plasma treatments used to bombard loose contaminants from the surface. Oxygen-based plasma is used to react with carbon to form gaseous CO & CO2.

Wire Bond Process Description

The substrate panel is fed from a carrier into the wirebond machine for setup where each bond pad location is loaded.
MAPBGA Transfer Mold and Cure

Transfer Mold Process Description
Substrate panels are loaded from a carrier into the heated mold tool. Mold pellets are loaded into the mold gate where clamp pressure is used to create a seal between top and bottom die around the substrate. Mold compound is transferred through the gate runners into the mold cavity.

Transfer Mold Cure Process Description
Molded substrate panel is then placed into a curing oven to complete the carbon cross linking process and to relieve internal mold stresses.
Laser Marking and Solder Ball Attach

Laser/Pad Marking Process Description
Molded substrate panels are then loaded into the laser marking machine from a carrier and marked to a defined set of criteria.

Solder Ball Attach Process Description
Molded substrate panels are loaded into the ball attach machine where pins in the exact ball array pattern are dipped into solder flux and placed on the substrate panel. A ball tool places the solder balls on the substrate panel. Substrate panels with solder balls then proceed through a multi-stage convection reflow oven. Each stage is set to defined temperature in order to meet a target reflow profile.
Flux Cleaning and Package Singulation

Solder Flux Clean Process Description
A flux clean step follows the reflow process utilizing heated de-ionized water.

Saw Singulation Process Description
Completed panels are then singulated by sawing the panel into individual units. High-pressure water is sprayed on the panel to help reduce the saw cut friction while also providing a final flux wash to remove any leftover residue.
Molded Array Process Overview

For PBGA, units are molded in individual cavities and punch singulated.

1. Multi-Up Organic Substrate Strip
2. Dispense Epoxy on Die Flag
3. Place Chip on Die Flag and Cure Epoxy, Plasma Clean
4. Wire Bc Plasma Clean & Wire Bond
5. Overmold and Cure
6. Flip Substrate and Place Fluxed Solder Balls
7. Reflow Solder Balls
8. Clean to Remove Residual Flux
9. Saw into Single Packages
Burn-In

The Bathtub Curve
Hypothetical Failure Rate versus Time

- Infant Mortality
- Decreasing Failure Rate
- Normal Life (Useful Life)
- Low "Constant" Failure Rate
- End of Life Wear-Out
- Increasing Failure Rate

Time

freescale™
Semiconductor Market Trends
World Semiconductor Market Slowing After Rapid Growth in 2010
2011 Grew +0.4%; 2012 Trending to -2 to -4%; 2013 expected ~5-6%

Source: WSTS, Sept’2012 and Freescale Internal Analysis
Semiconductor Market Historical Growth
World Semiconductor Market Revenues, Annual % Change

Average Growth 2001-2011: 8.0% per Year

Source: WSTS, Freescale Strategy, iSuppli, Gartner
Asia Pacific Continues To Gain in Semiconductor Market Regional Shares, With China the Single Largest Country for Shipments

Percent of Total Semiconductor Market

Source: WSTS
Semiconductor Content (Semi Revenues/Electronics) has flattened out over time

Source: IHS iSuppli, Q2’12; WSTS
Industry in Slowing Long-Term Growth Trend

Semiconductor Market Revenues in Billions of Dollars

<table>
<thead>
<tr>
<th>Years By Quarter</th>
<th>1970s</th>
<th>1980s</th>
<th>1990s</th>
<th>2000-06</th>
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</table>

Source: WSTS, Freescale Strategy, iSuppli, Gartner
Semiconductor End-Markets—2011
Auto Gained +1%, Communication Gained +3%; Consumer Lost -1%; Data Processing Lost -3% since 2010

No Significant Change in Industrial, Military % of Total Market

Source: WSTS, End Use Report
* Note: Communication includes Cellular & Infrastructure applications
Semiconductor Market By Product – 2011
MPU, Logic, Sensors, Optoelectronics & Discretes Grew Fastest

Share of Industry Total is shown in %
Source: WSTS, Jan’12
Automotive Semiconductor Market By Product – 2006

Overall Market

- Logic: 26%
- Analog: 14%
- Sensors: Opto: 6%
- Discretes: 2%
- MCU: 5%
- DSP: 3%
- DRAM: 12%
- Flash: 9%
- Other Memory: 2%

Automotive Market

- Logic: 24.3%
- Memory: 4.8%
- Discrete: 13.2%
- Analog: 12.8%
- Sensor: 10.2%
- Opto: 4.8%
- MCU: 29.8%

Source: WSTS, End Use Report
## Technology Offerings Across Markets

<table>
<thead>
<tr>
<th>Automotive</th>
<th>Industrial</th>
<th>Consumer</th>
<th>Wireless Handsets</th>
<th>Networking Infrastructure</th>
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<tbody>
<tr>
<td>Multimedia processors</td>
<td>Multimedia processors</td>
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<tr>
<td>Microcontrollers</td>
<td>Communication processors</td>
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<tr>
<td>Embedded microprocessors</td>
<td>Control processors</td>
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<tr>
<td>Wireless connectivity: baseband processing, RF transceivers, and power amplifiers</td>
<td>RF, PA and baseband</td>
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<tr>
<td>Sensors</td>
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<tr>
<td>Analog &amp; power management</td>
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<tr>
<td>Digital signal processor technologies</td>
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</tbody>
</table>
Automotive Product Cycles vs Other Semiconductors

How to make automotive golden years attractive
Volume: individual parts & overall market?

Factory Closure or Obsolete Technology

Customer Qual Cycle (2-3 years)
Drivers for Semiconductor Fabrication Process Change
Effect of Process Shrink: NVM Bitcells

Scale Drawing

- MC68HC11 → EEPROM
- MC68F333 → 1.5T Flash
- MPC565 → MPC5554
- MPC5554 → 130nm
- 130nm → ETOX Flash
- ETOX Flash → High Density
- MPC565 → ETOX Flash
- ETOX Flash → High Density
- MPC555 → 1T Flash
- 1T Flash → High Density

NXP
freescale™
Freescale 1T Flash Bit Cells at 0.35µm and Below

CDR1 0.35µm  
FN/FN 1T  
2.7µm²

CDR3 0.25µm  
HCl/FN 1T  
0.995µm²

HiP7 130nm  
HCl/FN 1T  
0.359µm²

CMOS90  
HCl/FN 1T  
0.18µm²

CMOS55  
HCl/FN 1T  
<0.15µm²

CMOS40  
HCl/FN 1T  
< 0.1µm²

All bitcells are drawn on the same scale.
Process Change for Microcontrollers

MPC555
Black Oak
CDR1 0.35u
448K Flash
7 million transistors

MPC565
Spanish Oak
CDR3 0.25u
1MB Flash
14 million transistors

MPC5554
Copperhead
HIP7 0.13u
2MB Flash
34 million transistors
Process Change for Analog ICs

- 8 Output Switch
  - 0.375 ohm
  - SMARTMOS 2.5

- 16 Output Switch
  - 0.375 ohm
  - SMARTMOS 5AP
Total Cost of Ownership

- Frequency
  - Test time
  - EMC components
- Package
  - Machinery
  - Board size
  - Capital equipment
  - Tier 1 volume

Silicon $ + Tier1 $ = Micro $
Quality and Failure Analysis
Screening Techniques for Zero Defects

**BMY (Below Minimum Yield)**
- Screen wafers with lower than statistical distribution of yield

**SBL (Statistical Bin Limits)**
- Screen wafers with unusual bin signatures

**Static PAT (Process Average Testing)**
- Screen die with parametrics that are outside statistical distribution

**GDBC (Good Die Bad Cluster)**
- Screen die with failing neighbors

**Dynamic PAT**
- Screen die with parametrics that are outside the wafer distribution
**Statistical Bin Limits/ Process Average Test**

**SBL (Statistical Bin Limits)**
- SBL contains outlier wafers in Freescale and provides faster feedback on slight process/tool anomalies causing higher bin fallout

**Bin Limit Setting:**
- Ensure all wafers with unusual bin signatures are flagged and held for disposition
- K is set between 4 and 8 for critical bins:
- Bins with very low fallout are set at fixed level to detect excursions
- Limits are reviewed every 3-6 months (Product Volume Dependent)

**Calculation:**
SBL = Median + K*Robust Sigma

**Static PAT**
- Statistical test limits are set in the probe program to screen outlier die.
- Limits are reviewed every 3-6 months (Product Volume dependent)
Good Die Bad Cluster (GDBC)
Defect isolation in a semiconductor device uses the same troubleshooting methodology to isolate a failure in any large system.

- The problem description is first described at the system level (Die level failure description)
- Data is collected to isolate the failure to a sub system (Functional Blocks within a device)
- Analysis continues, eliminating all the possible causes until the source of the failure is identified
Known Good Die (KGD) analysis samples are typically returned to Freescale still attached to the target application. The die must be removed and packaged for analysis and protection of the die. Due to the fragile nature of the die, a visual inspection is performed at each step to ensure device integrity.

- **Step 1: Die Removal**
  - Wirebonds pulled
  - Die encapsulation in epoxy
  - Customer’s board is milled down from the backside until the die is freed from the target application
  - Die removed from epoxy encapsulant

- **Step 2: Die Packaging**
  - Epoxy is removed from the die
  - The die is glued to a PBGA (Plastic Ball Grid Array) substrate.
  - Device is wirebonded to the correct pin-out configuration
  - Plastic mold compound is used to encapsulate the device
  - Solder spheres are attached to bottom of the package substrate.

The die extraction and re-packaging process typically takes 4-7 days, dependent on the condition of the device upon receipt.
Freescale Failure Analysis Flow: Phase 2 - Electrical Verification

• Step 1: Device level testing
  - Device is evaluated on the bench using an EVB (Evaluation board) using standard evaluation tool to assess basic functionality.
  - Device tested to the production test program on Automatic Test Equipment (ATE) across temperature and voltage.
  - Test results are compared to the customer reported failure description for correlation.

• Step 2: Historical Database search
  - Freescale data base is reviewed to determine any potential lot issues
  - Test results compared to the return history to determine if the test results correlate with a known failure mechanism (Signature Failure Analysis)
After completion of the electrical verification, the device is submitted to the Product Analysis Lab.

Verification/Failure Mode Characterization (1-2 Days)
- Duplicate reported Failure Mode found in physical analysis lab compared to correlation device.
- Decapsulation (removal of top of plastic package to expose die surface) / Visual Inspection
- Optical inspection of area associated with observed Failure Mode
- Confirm failure mode is unchanged after decapsulation
- Data is collected on the failing device as well as a known good samples.

Electrical Isolation (1 day – 4 weeks)
- Step 1: “Non-destructive” isolation
  - Light Emission microscopy – Infrared light camera is used to capture anomalous IR emission sites.
  - Liquid Crystal – a temp. sensitive solution that changes color with temp.
  - OBIRCH (Optical Beam Induced Resistance Change) – a laser is scanned across the die surface to identify anomalous resistance points on the die. (See figure on the right)

- Step 2: Microprobe
  - In-circuit measurement technique that uses very fine wires to collect parametric data (signals Voltages, Resistances,)
  - Similar to using a multi-meter to troubleshoot an electrical system.
  - Requires microscopic holes to be drilled in the silicon order to access nodes of interest.
Typical EOS Failure
In order to collect data via microprobe, the Analyst needs to be able to access various circuit nodes within the die. A FIB (Focused Ion Beam) is used to drill sub-micron holes and:

- Conceptually can be thought of as an electric knife or a microscopic Mill/Drill. Removal rate is measured on the order of molecules.

Micro probing is an iterative process, and can require multiples FIB edits to collect the data needed to isolate the failing circuit element. Each FIB edit can take ~ 1 day to complete.

FIB can also be used to cut metal interconnects in order to isolate circuit elements.
Freescale Failure Analysis Flow:
Phase 3 – physical Isolation, Deprocessing

Once the analyst has isolated the failure to a single circuit element, physical analysis begins. There is no turning back once physical analysis begins as the device will no longer be functional.

There are 2 primary physical analysis techniques;
1. Layer by layer deprocessing
2. Cross – section.

Microprobe complete and failure isolated.
Deprocessing is deemed the best method

De-process layer by layer. Each layer at the failing location is inspected with a Scanning Electron Microscope (SEM)

Deprocessing Complete
Typically 1-5 days to complete
Freescale Failure Analysis Flow:
Phase 3 – Physical Isolation, Cross-Sections

- The FA analyst can also perform a cross section of a suspect circuit element.
- A very thin sample is cut out of the die using the FIB tool.
- Transmission Electron Microscopy (TEM) is used to look “through” the sample to identify a defect.
- Sample Prep and TEM completion can take 3-5 days.
Freescale Manufacturing
# Freescale Asset Light Strategy

## Flexible Sourcing
- Exit 150mm
- 200mm Internal/External
- 300mm External

## Invest in Differentiating Technologies
- eNMV Sensors
- SmartMOS/Analog RF

## Flexible Sourcing
- Auto, Industrial, Networking Int/External
- Consumer External Burn-in External

## Invest in Differentiating Technologies
- Power Analog
- High Performance Networking assembly and test
- Automotive sensor test
Freescale Semiconductor Global Sites

- **Freescale Chandler Fab – 8”**
  Chandler, AZ

- **Freescale Oak Hill Fab – 8”**
  Austin, TX

- **Freescale Austin Technology & Manufacturing Fab – 8”**
  Austin, TX

- **Freescale Tianjin Final Manufacturing**
  Tianjin, China

- **Freescale Kuala Lumpur Final Manufacturing-Kuala Lumpur**
  Kuala Lumpur, Malaysia
Manufacturing Partners

- TSMC, UMC, ASE, Amkor, Global Test
- Amkor, ASE, StatsChipPac
- Global Foundries, UMC, StatsChipPac
- Die Manufacturing
- Probe, Assembly & Test
Manufacturing Summary

• **Continue Our Strategy**
  - Flexible Manufacturing: The Right Model

• **Key priorities**
  - Customer Success
  - Quality
  - Best Cost
  - Asset Utilization
  - Flexibility & Assurance of Supply
## Flexible Sourcing on High-Growth Technologies
Planning for the Future

<table>
<thead>
<tr>
<th>Technology</th>
<th>Internal</th>
<th>External</th>
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<tbody>
<tr>
<td>0.25um Embedded Flash</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td>0.25um Analog/Hi Voltage</td>
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<td>0.18um Embedded Flash</td>
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<td>0.13um Embedded Flash</td>
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## Leveraging Our Foundry Relationships

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<tr>
<th>External Foundries</th>
<th>Locations</th>
<th>Key Technologies</th>
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<tr>
<td>TSMC</td>
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<td>Malaysia</td>
<td>Standard Linear, MOS Capacitors</td>
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<td>GaAs</td>
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## Assembly & Test Manufacturing Partners

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<td>KES</td>
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<td>Final Test and Burn-in</td>
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Questions?